

FIG. 1A

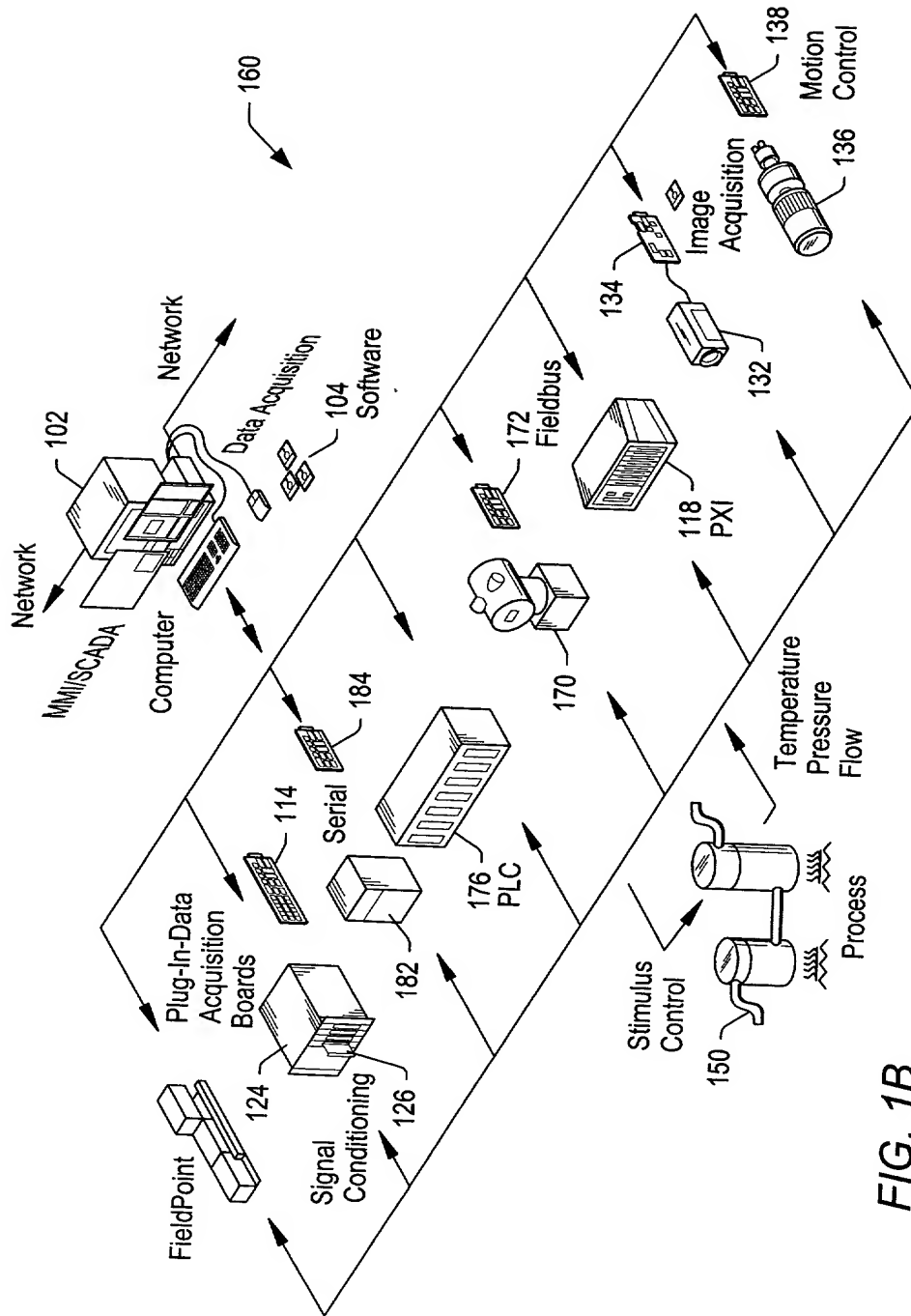


FIG. 1B

20182220" 26/8000T

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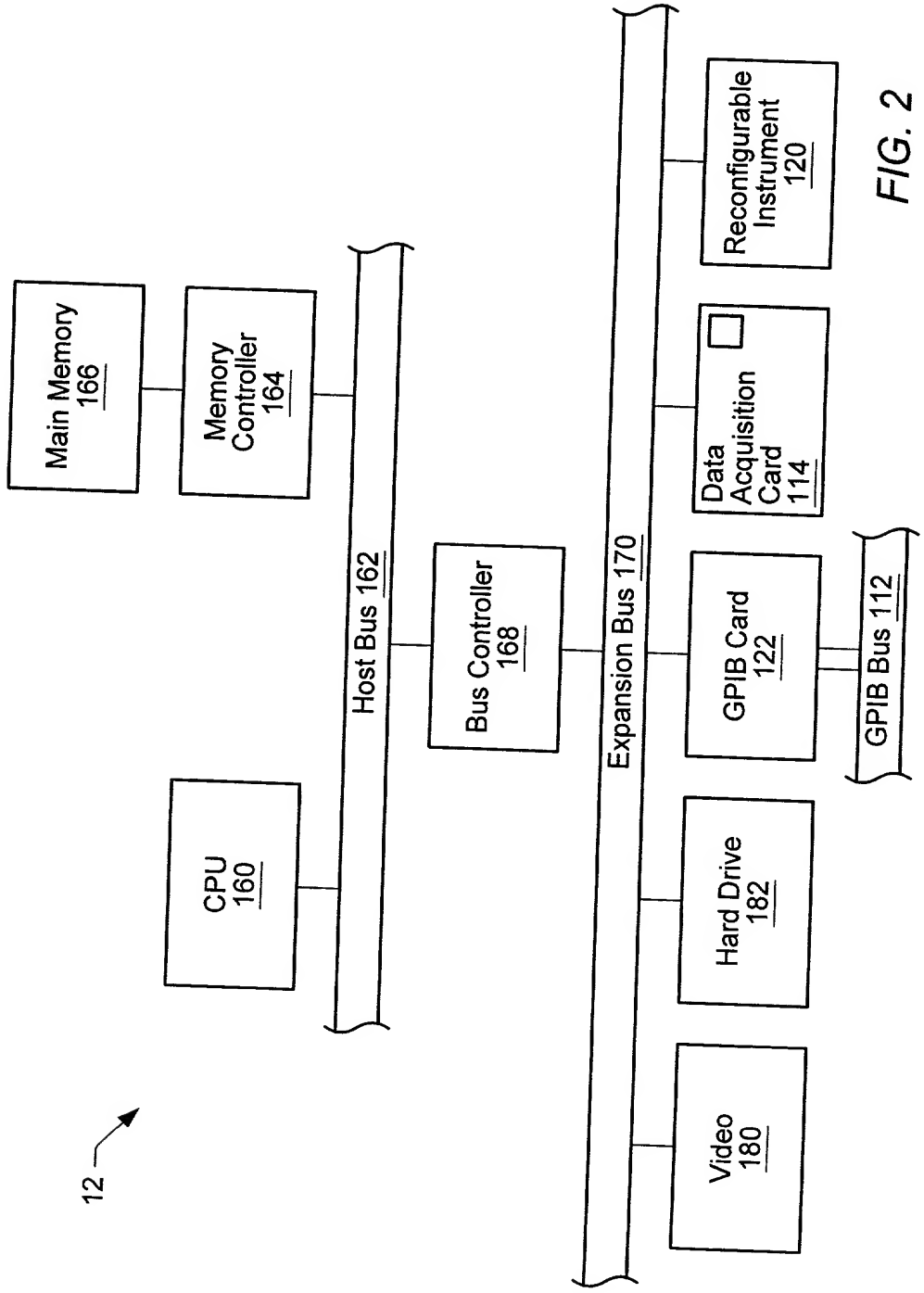


FIG. 2

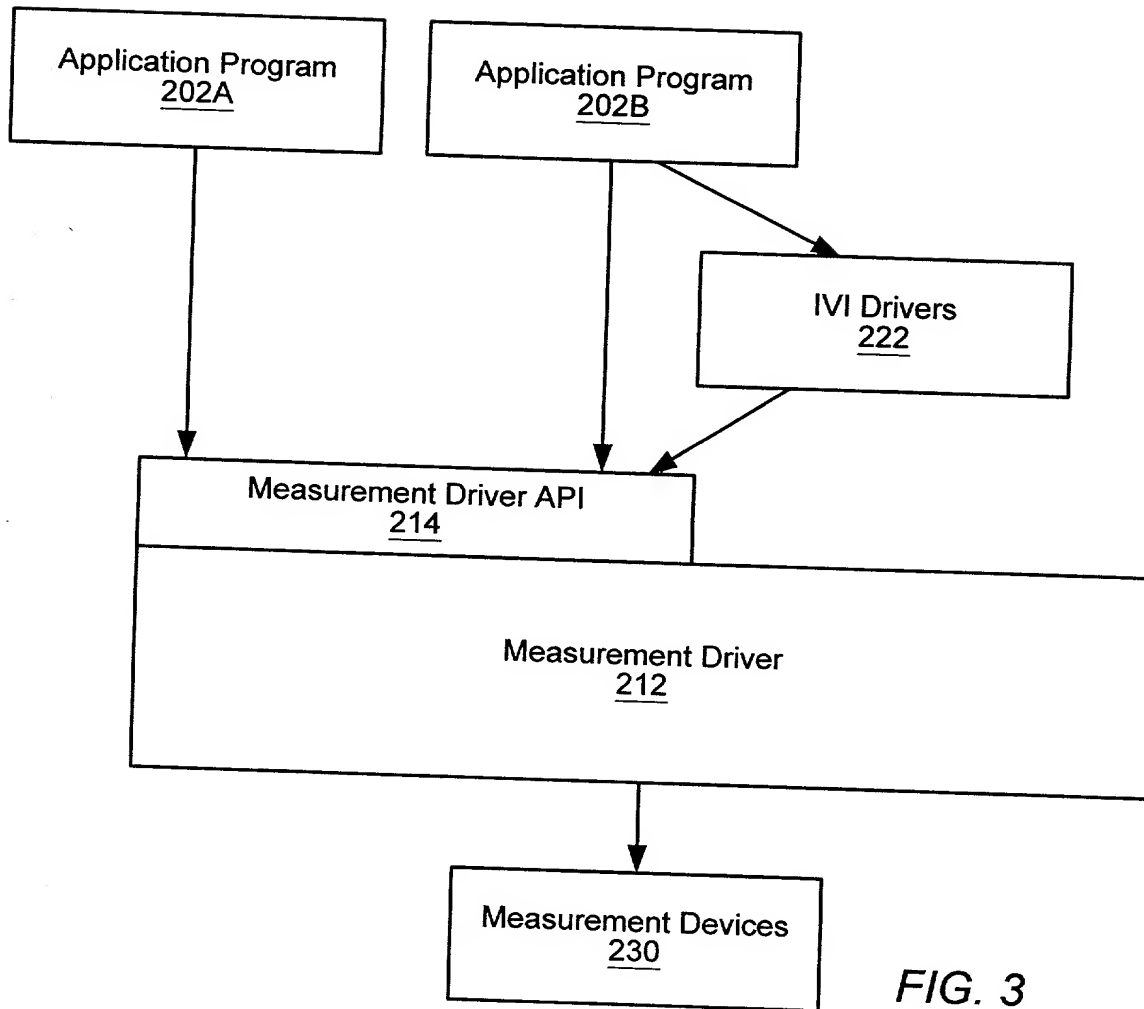


FIG. 3

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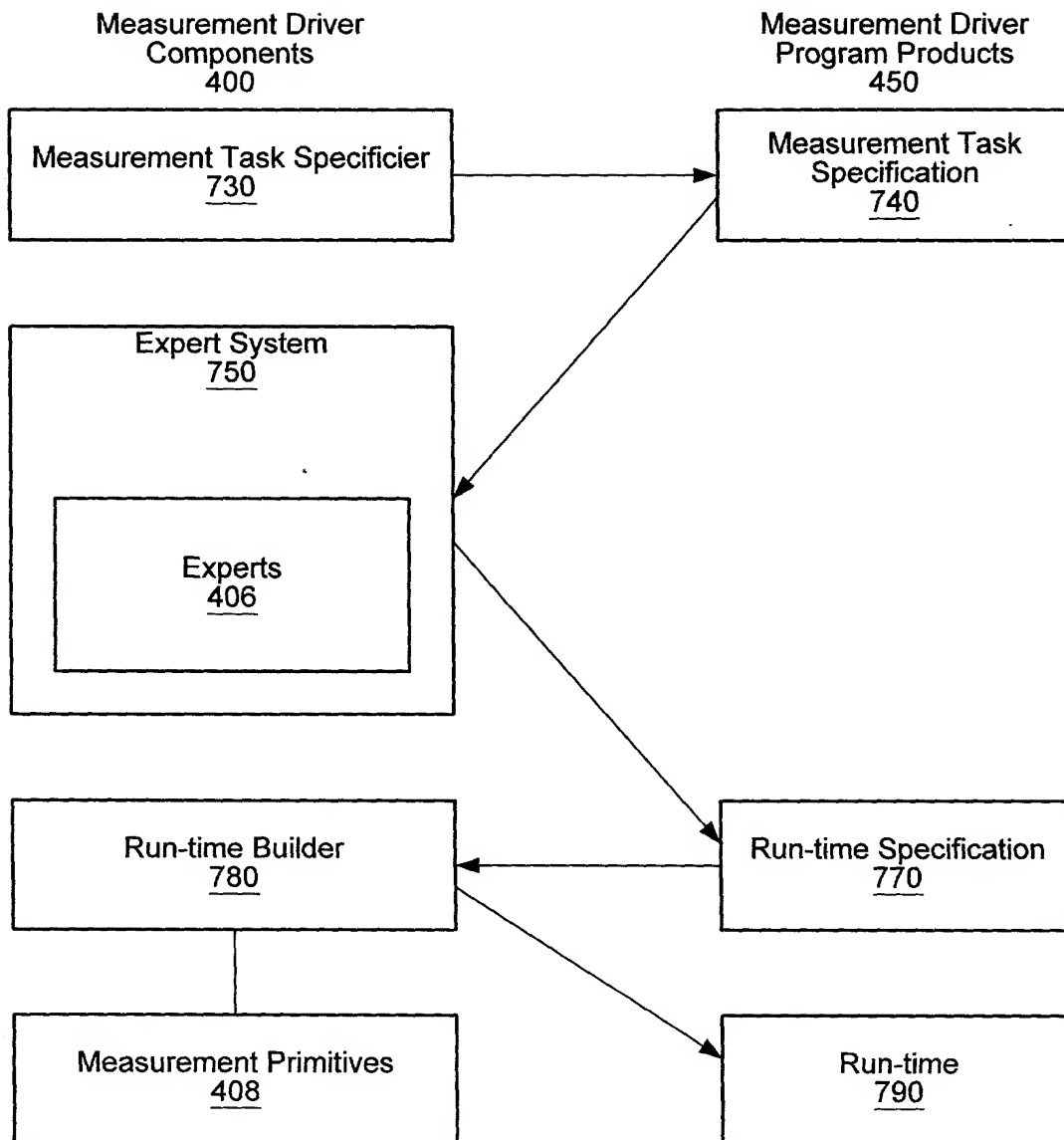


FIG. 4

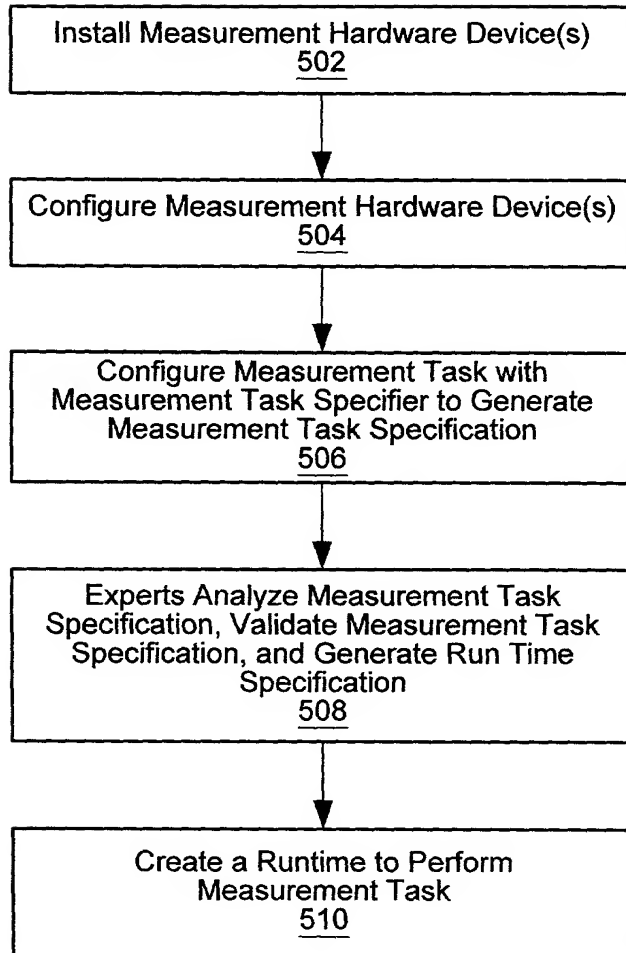


FIG. 5

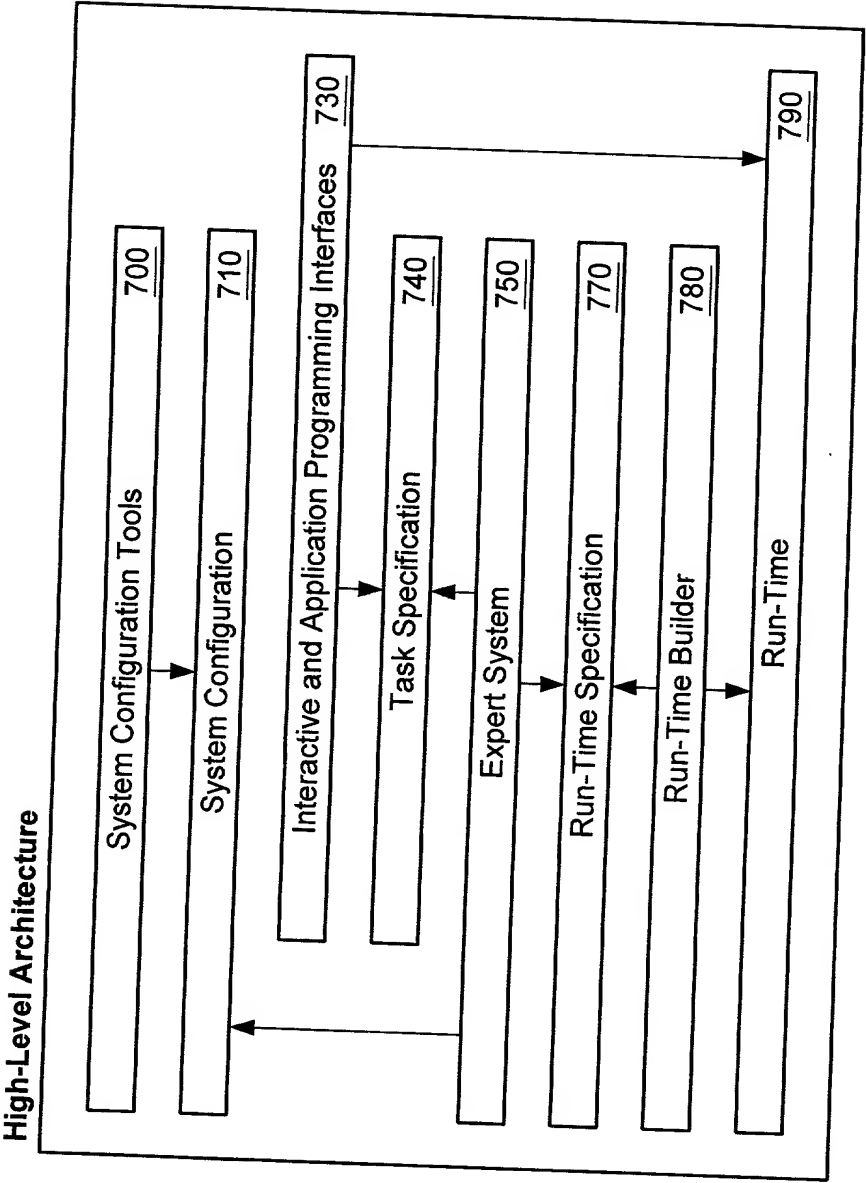


FIG. 6

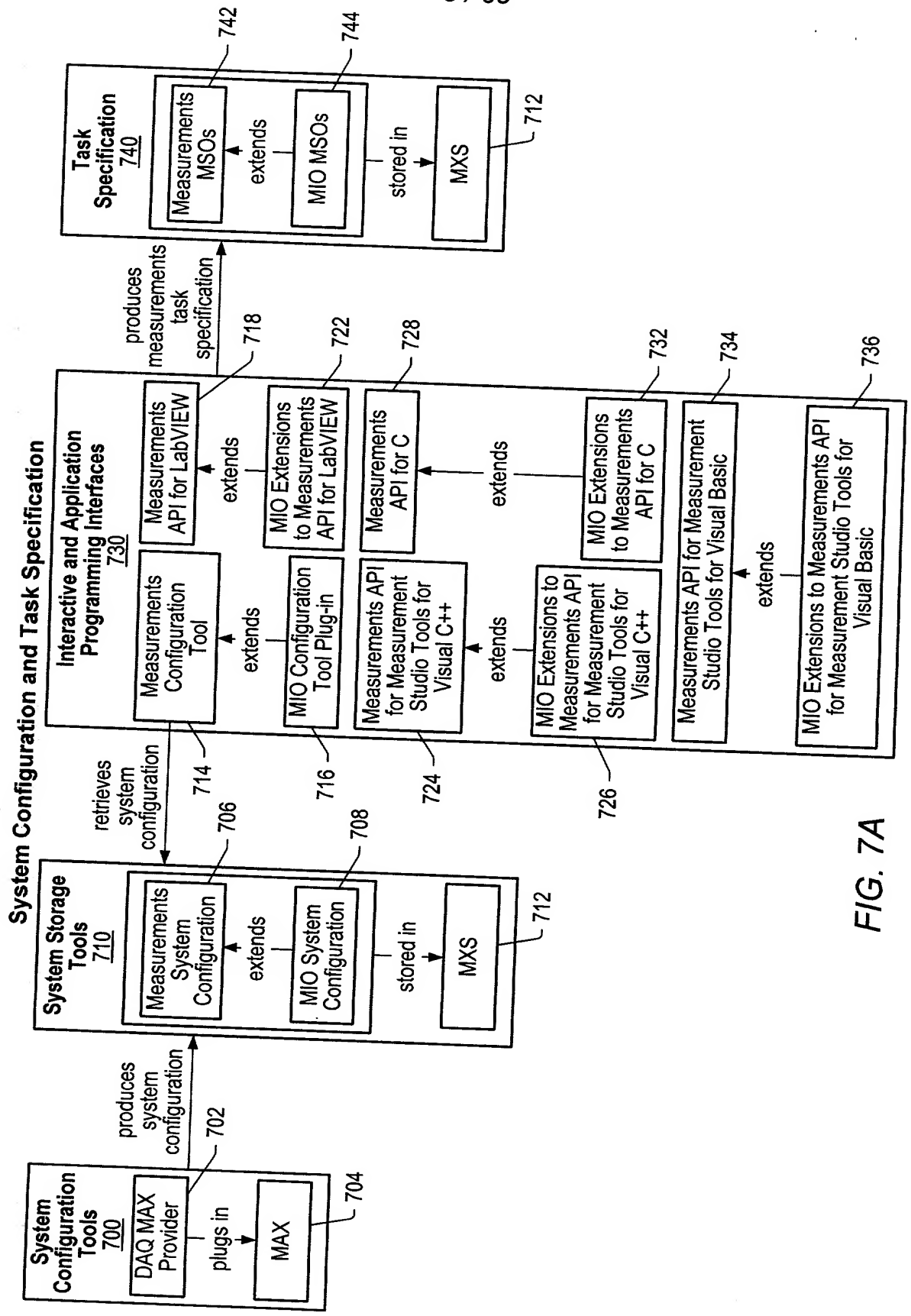


FIG. 7A

Compiling Task Specification to Task Run-time Specification

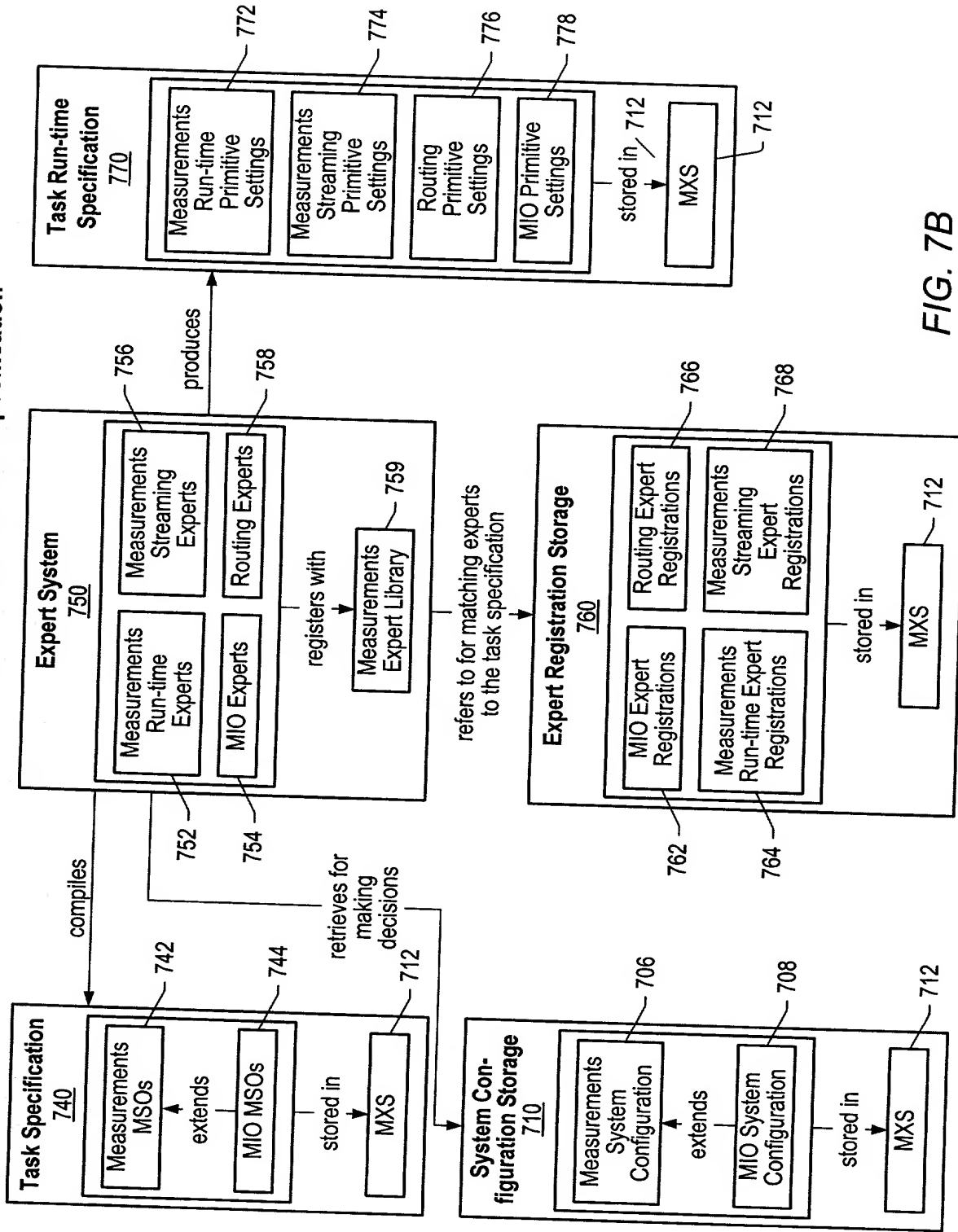


FIG. 7B

Building Task Run-time from Task Run-time Specification

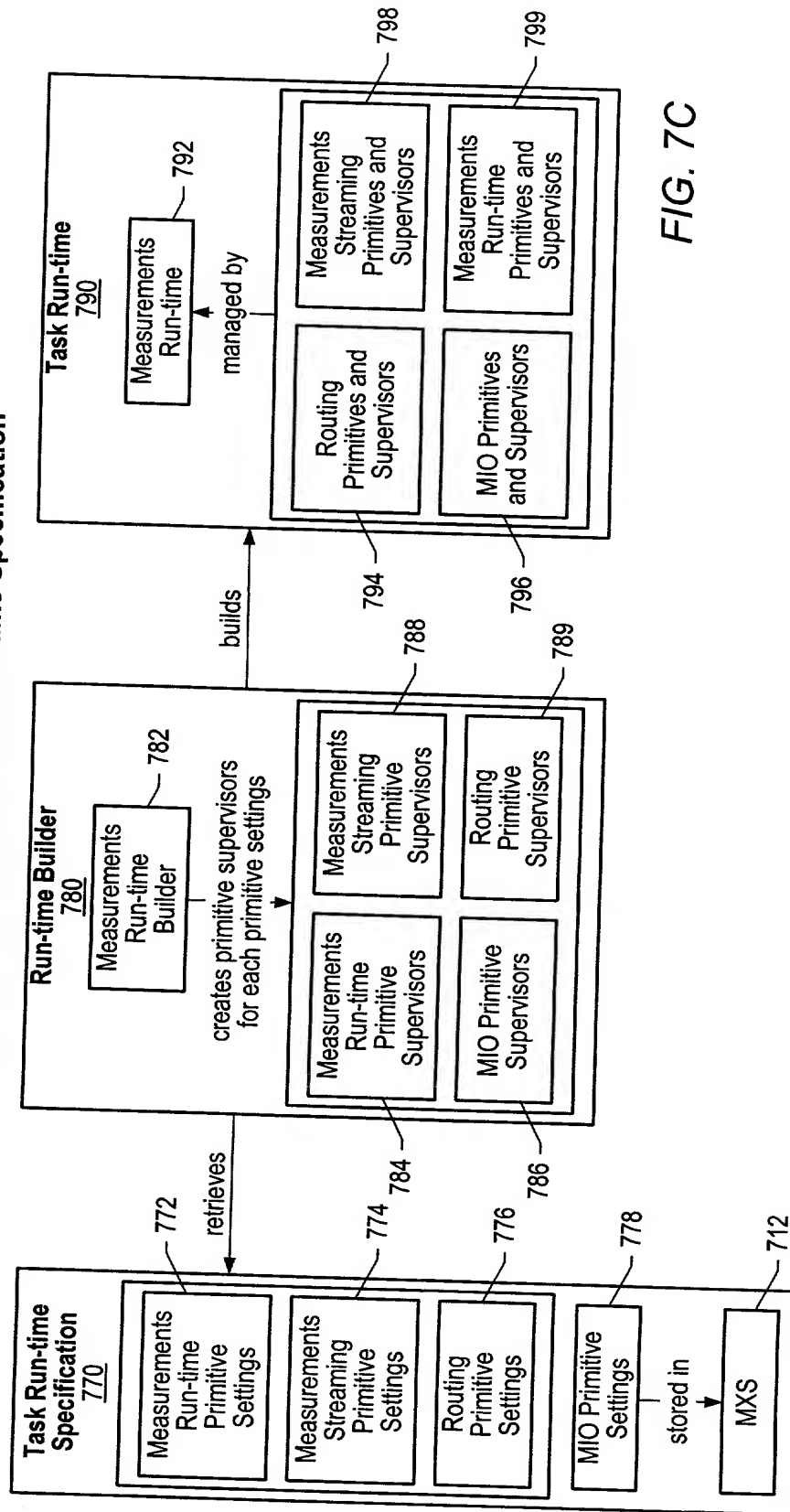


FIG. 7C

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Executing Tasks

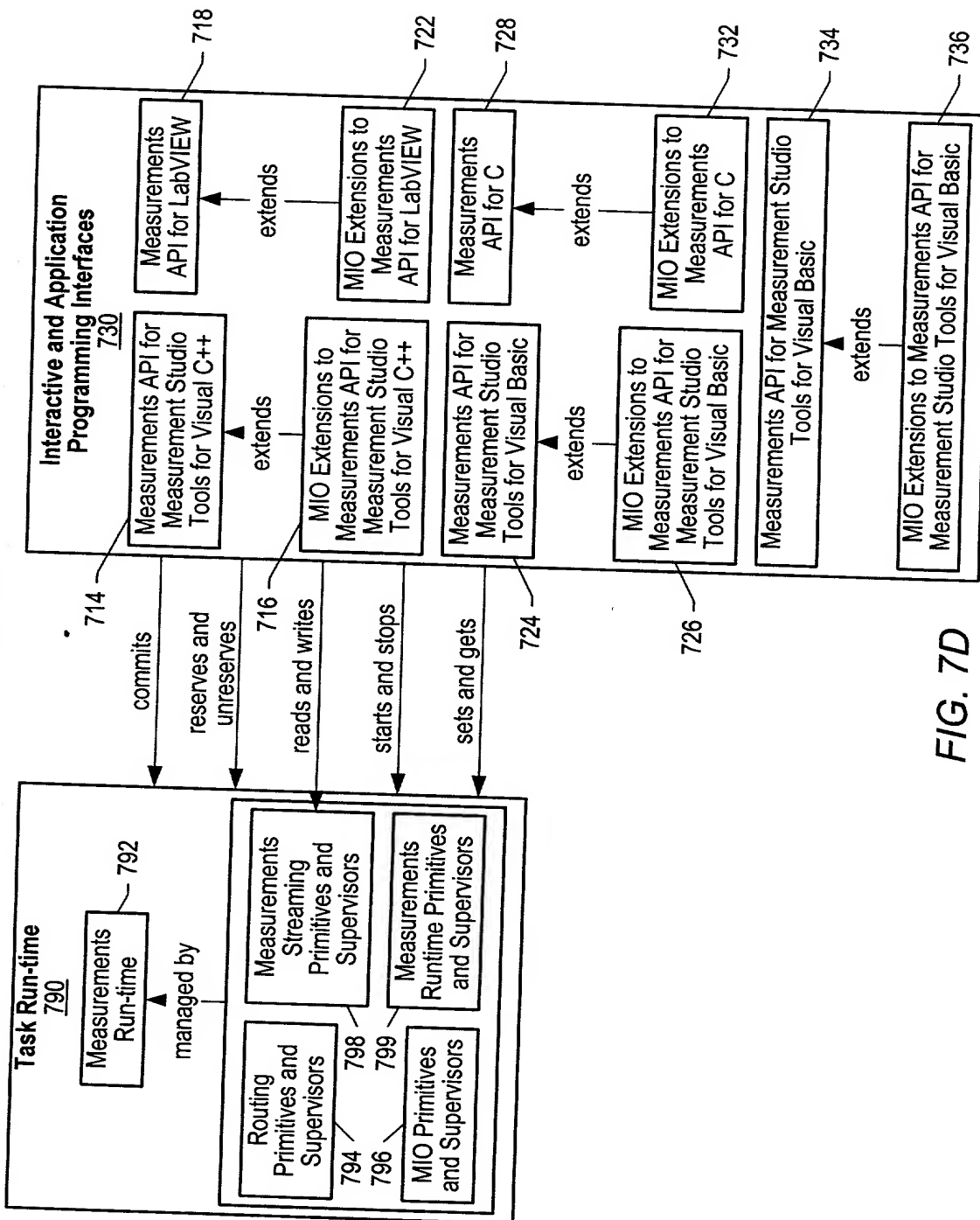


FIG. 7D

Packages for System Configuration and Task Specification

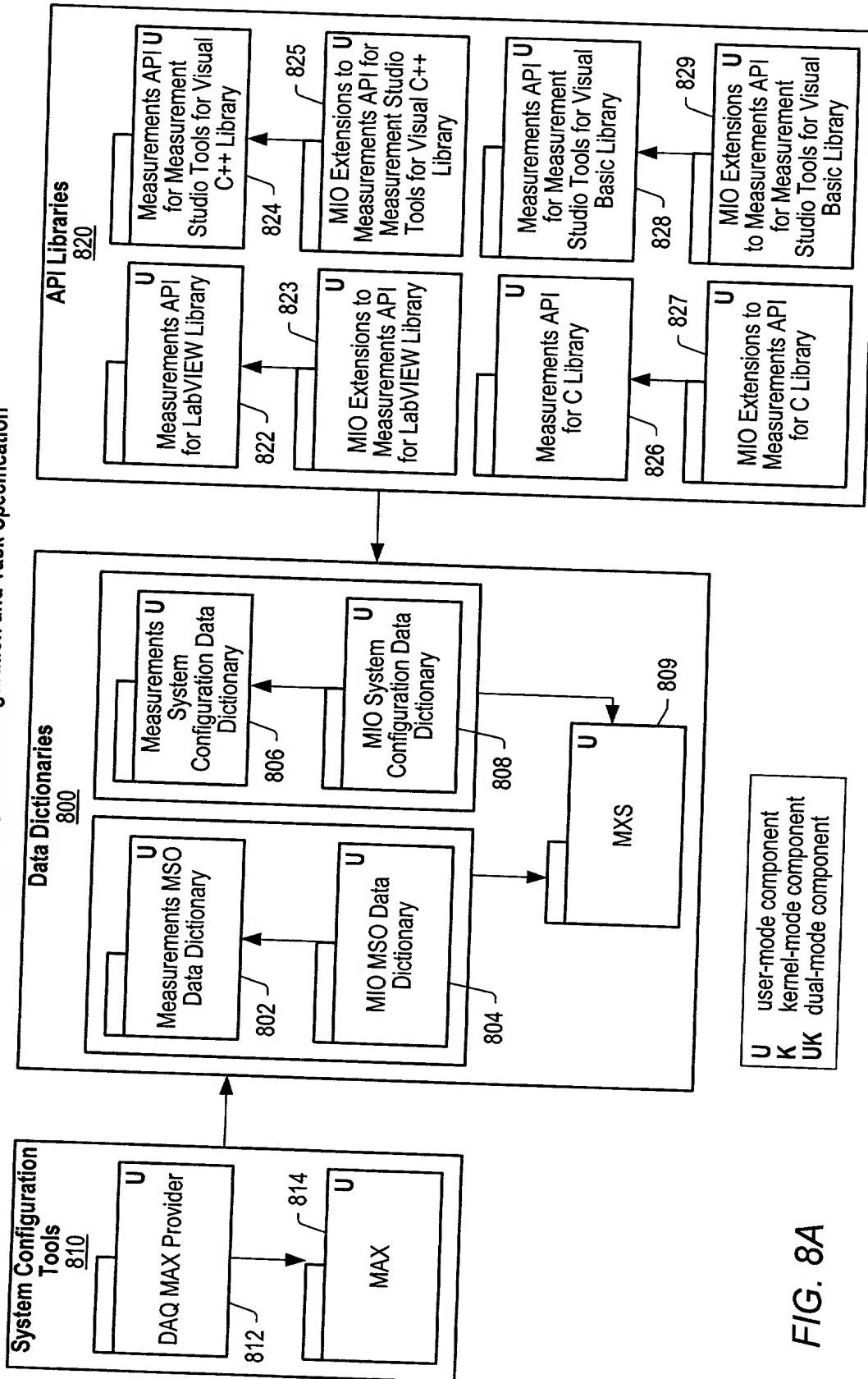


FIG. 8A

Packages for Compiling Task Specification to Run-time Specification

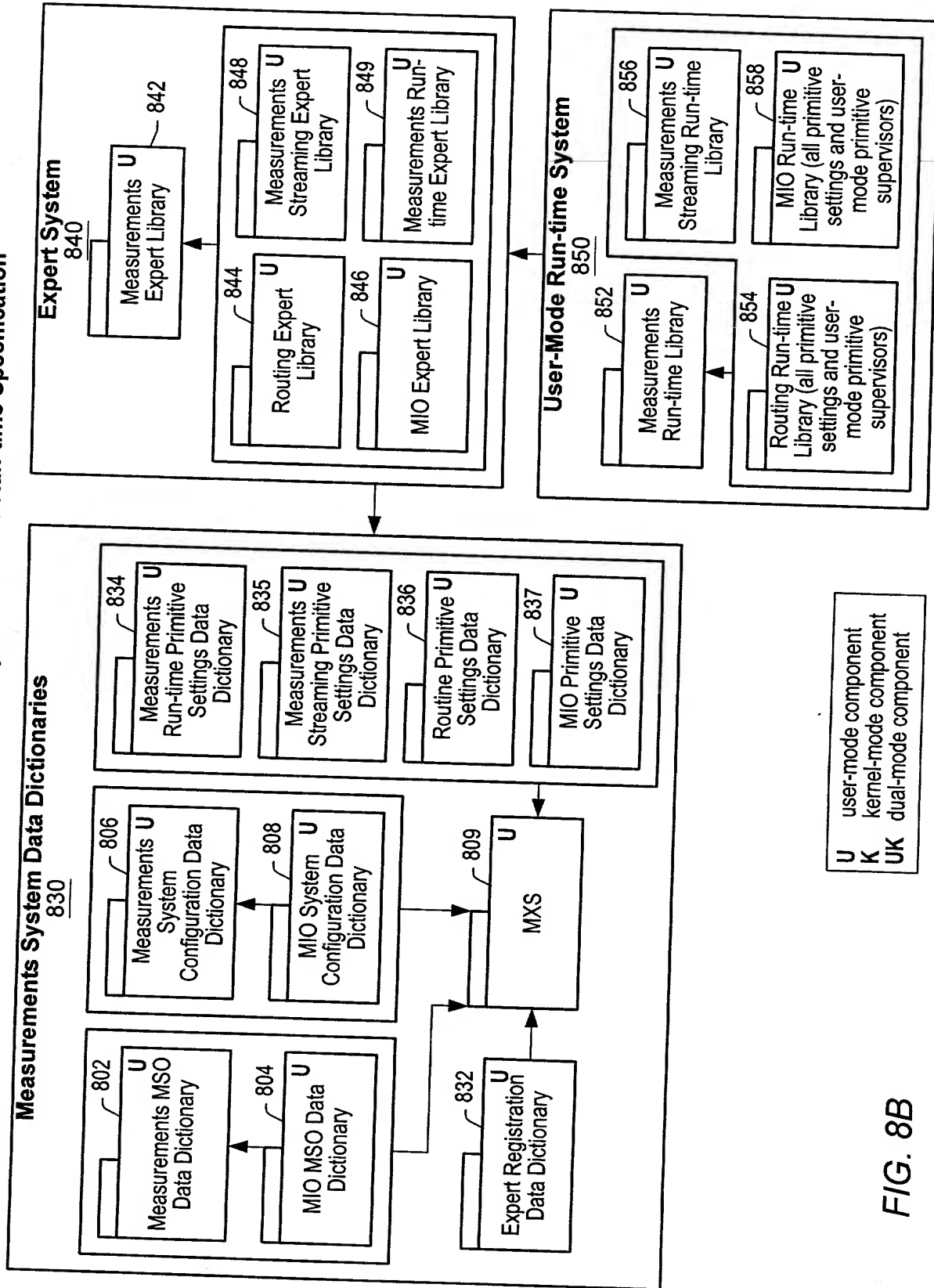


FIG. 8B

Packages for Building Task Run-time from Run-time Specification

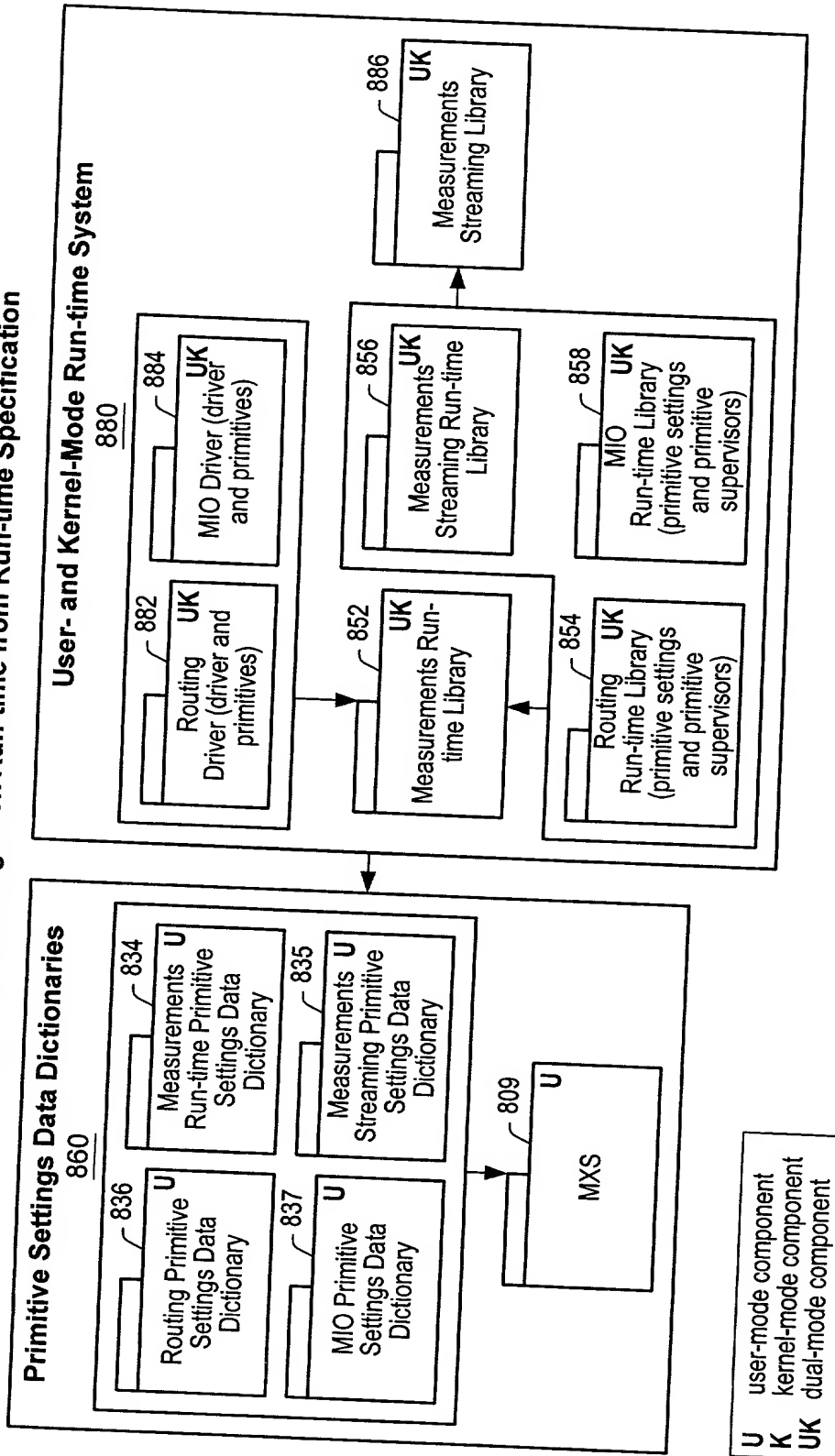


FIG. 8C

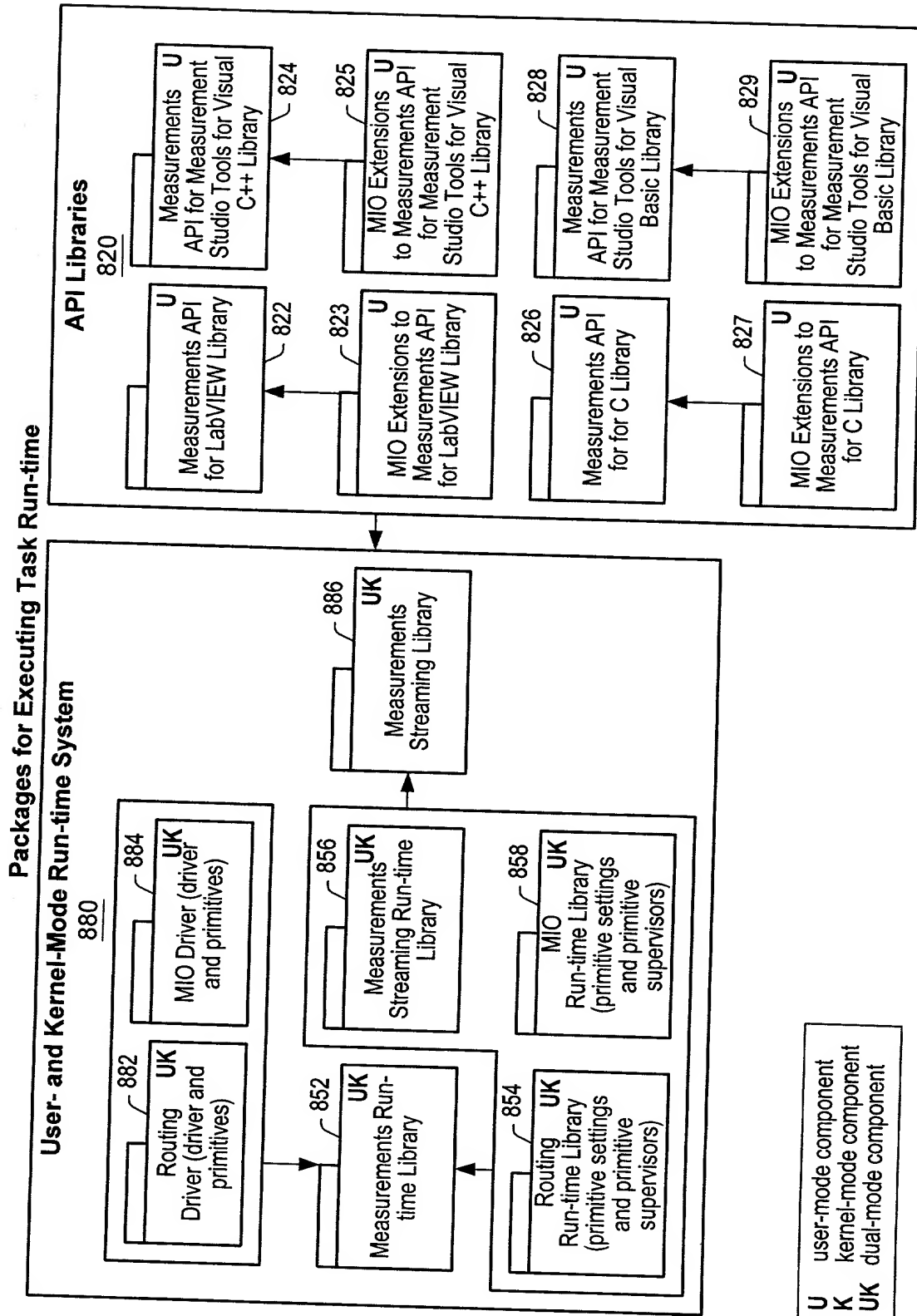


FIG. 8D

State Diagram for Measurement Tasks

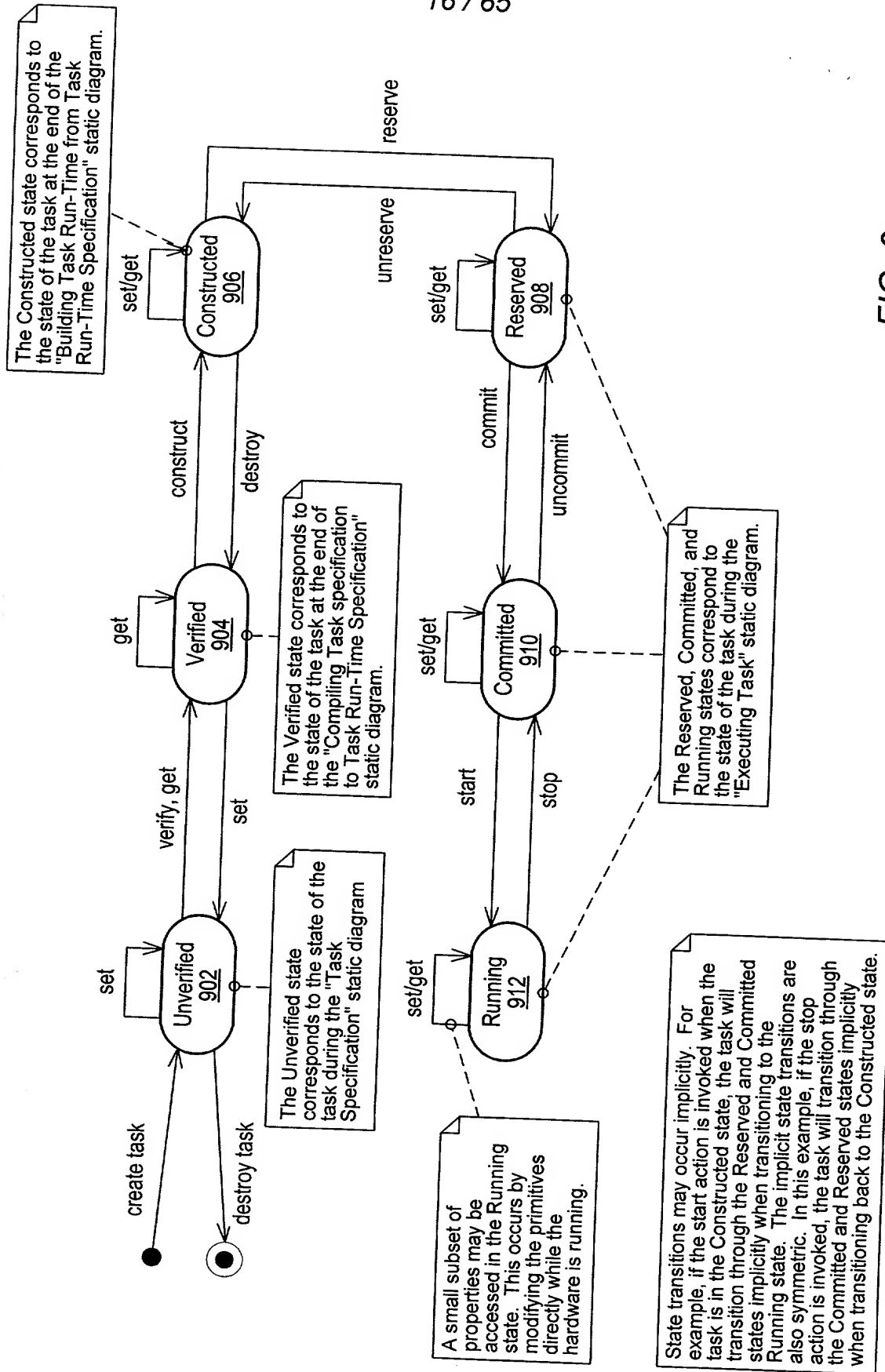


FIG. 9

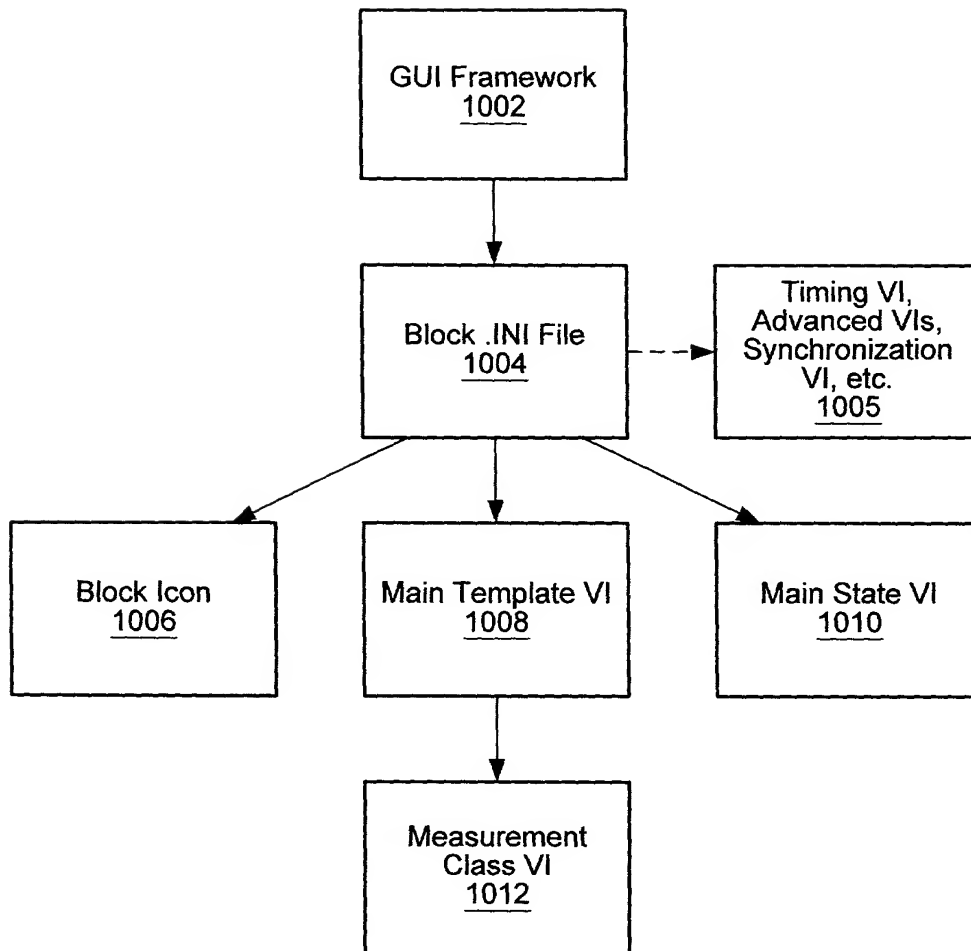


FIG. 10

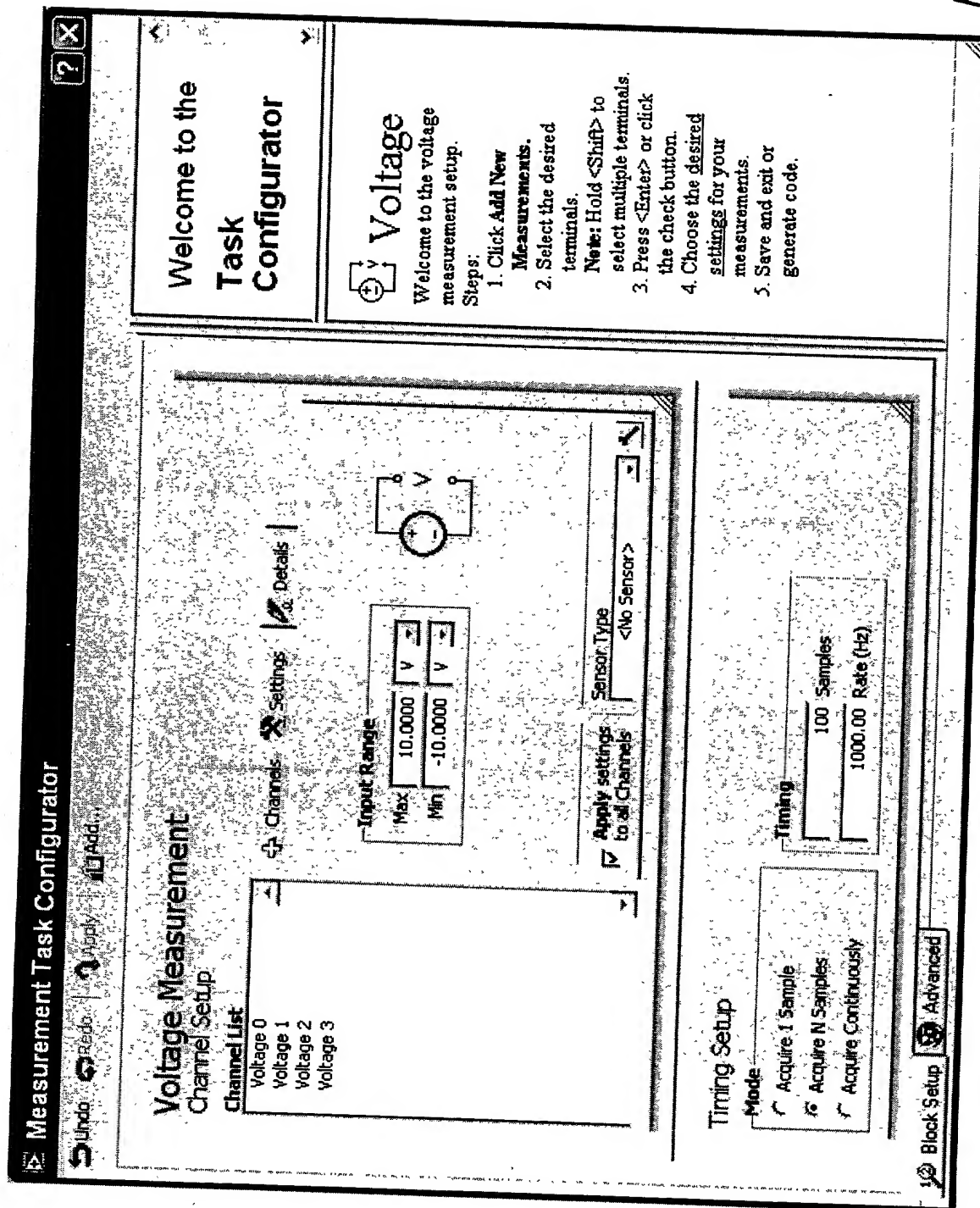


FIG. 11

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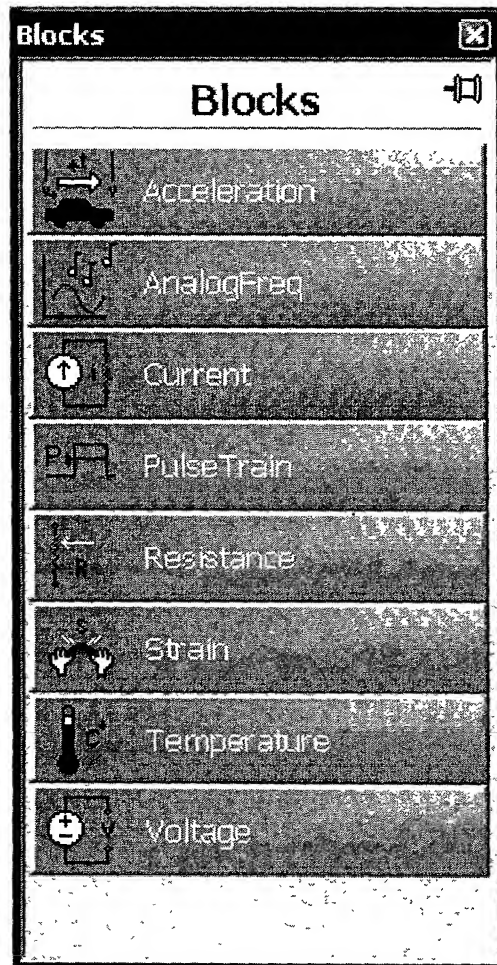


FIG. 12A

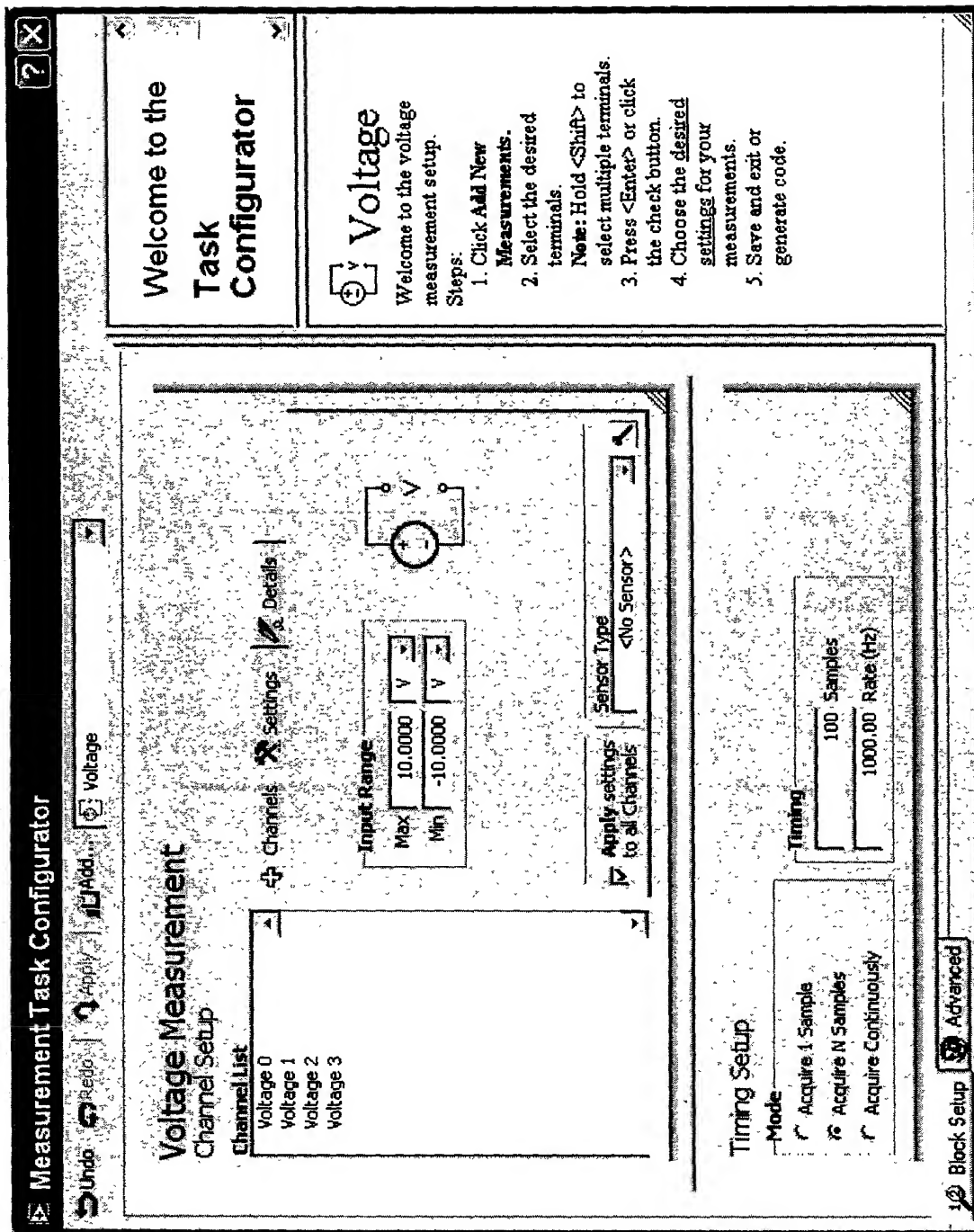


FIG. 12B

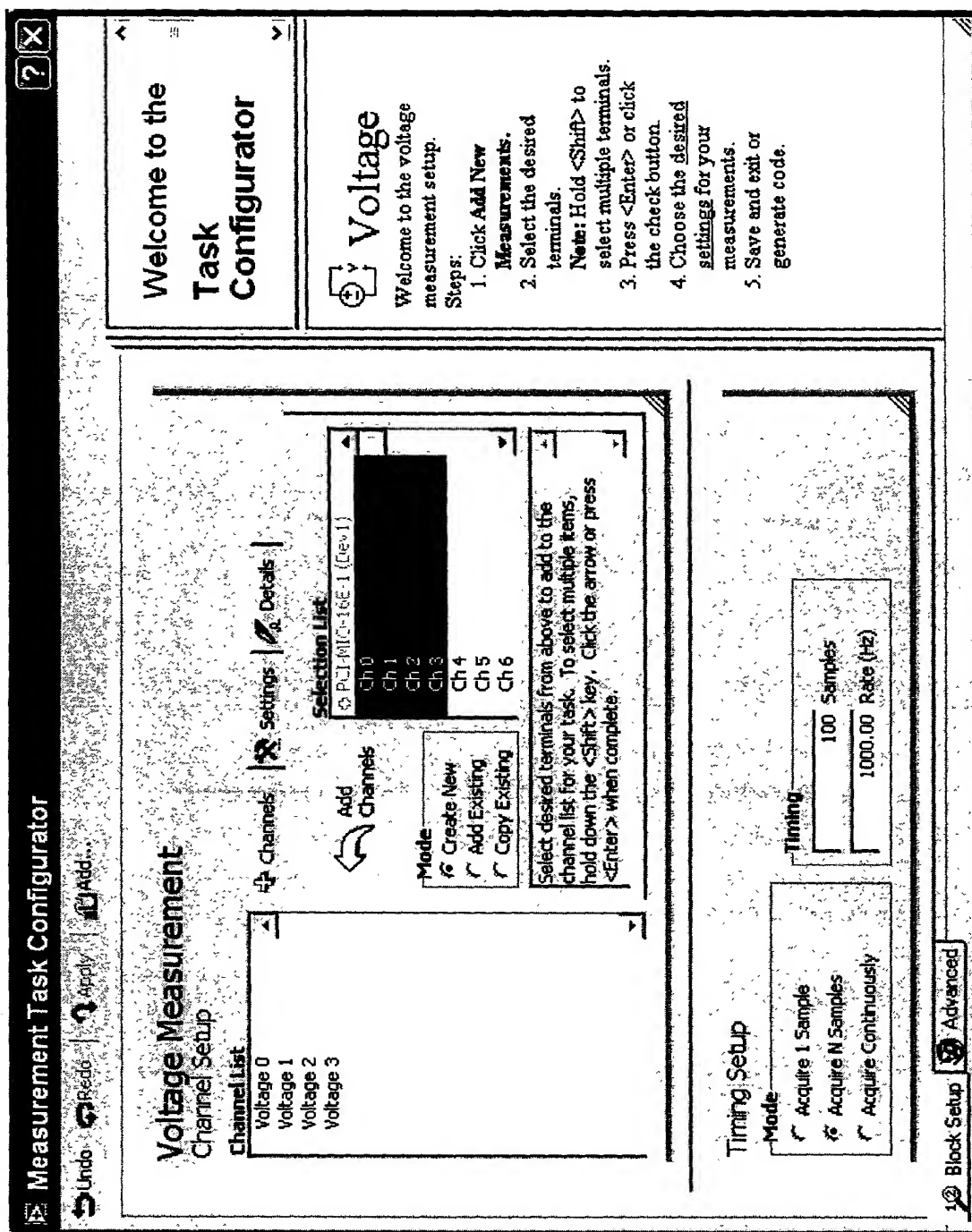


FIG. 12C

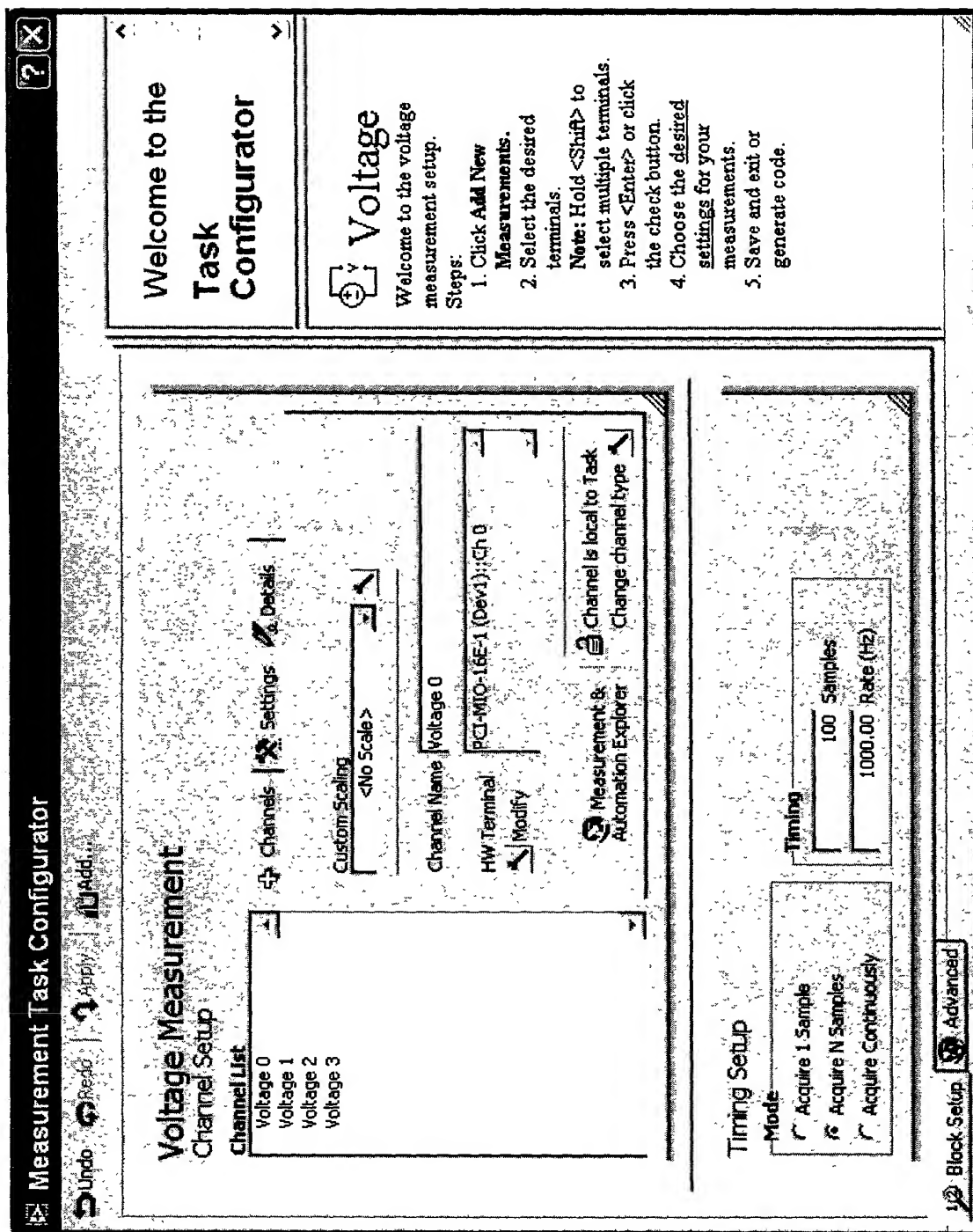


FIG. 12D

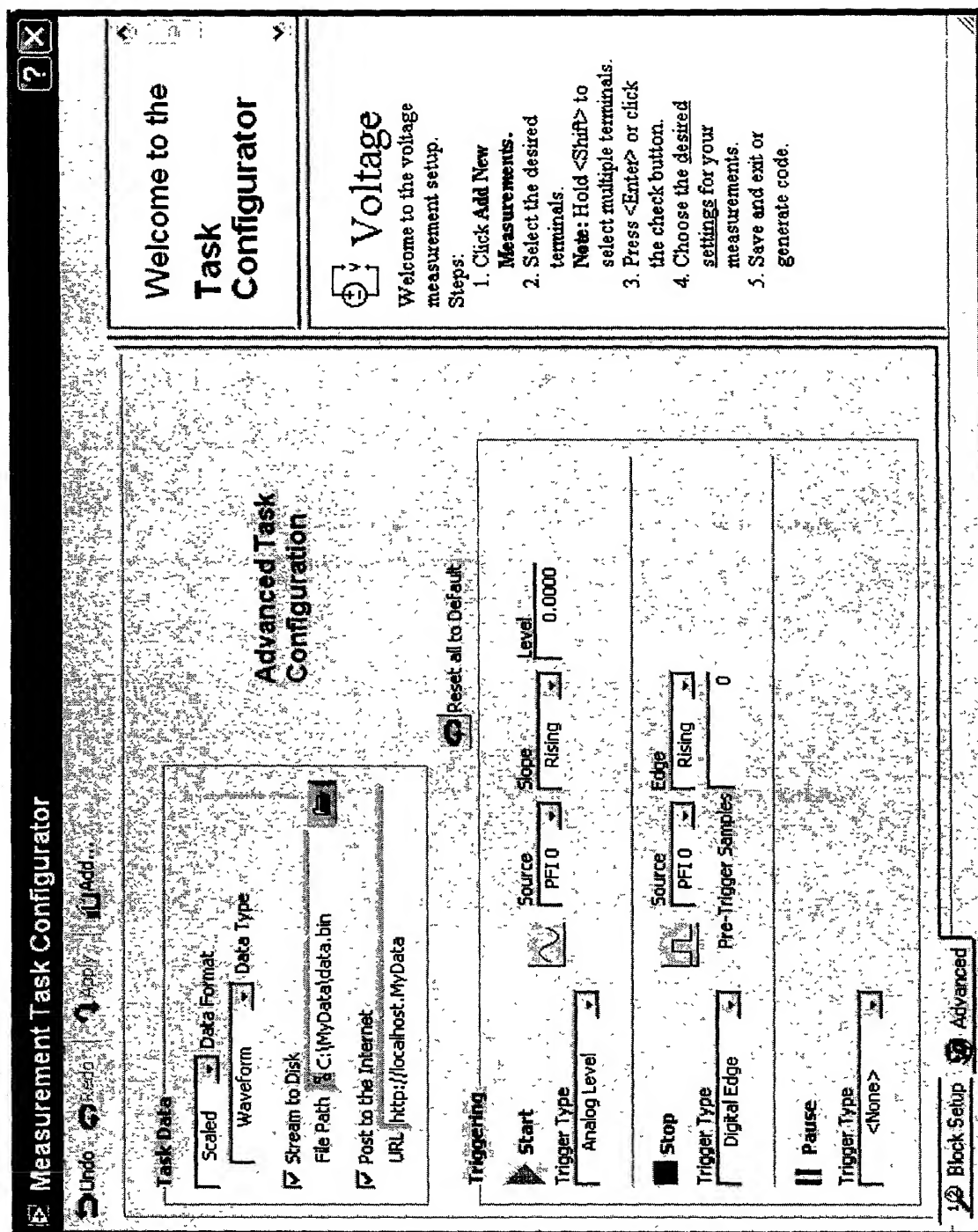


FIG. 13

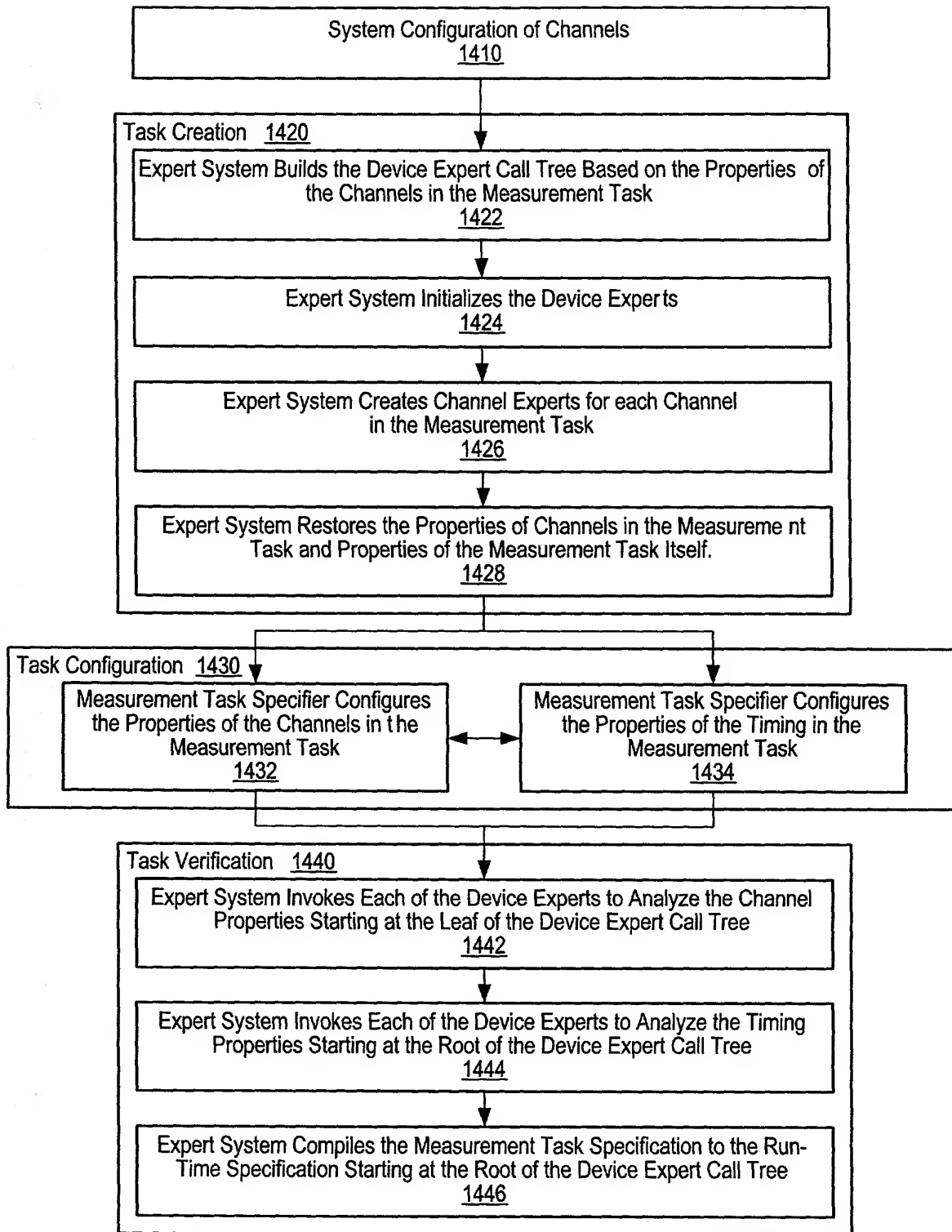


FIG. 14

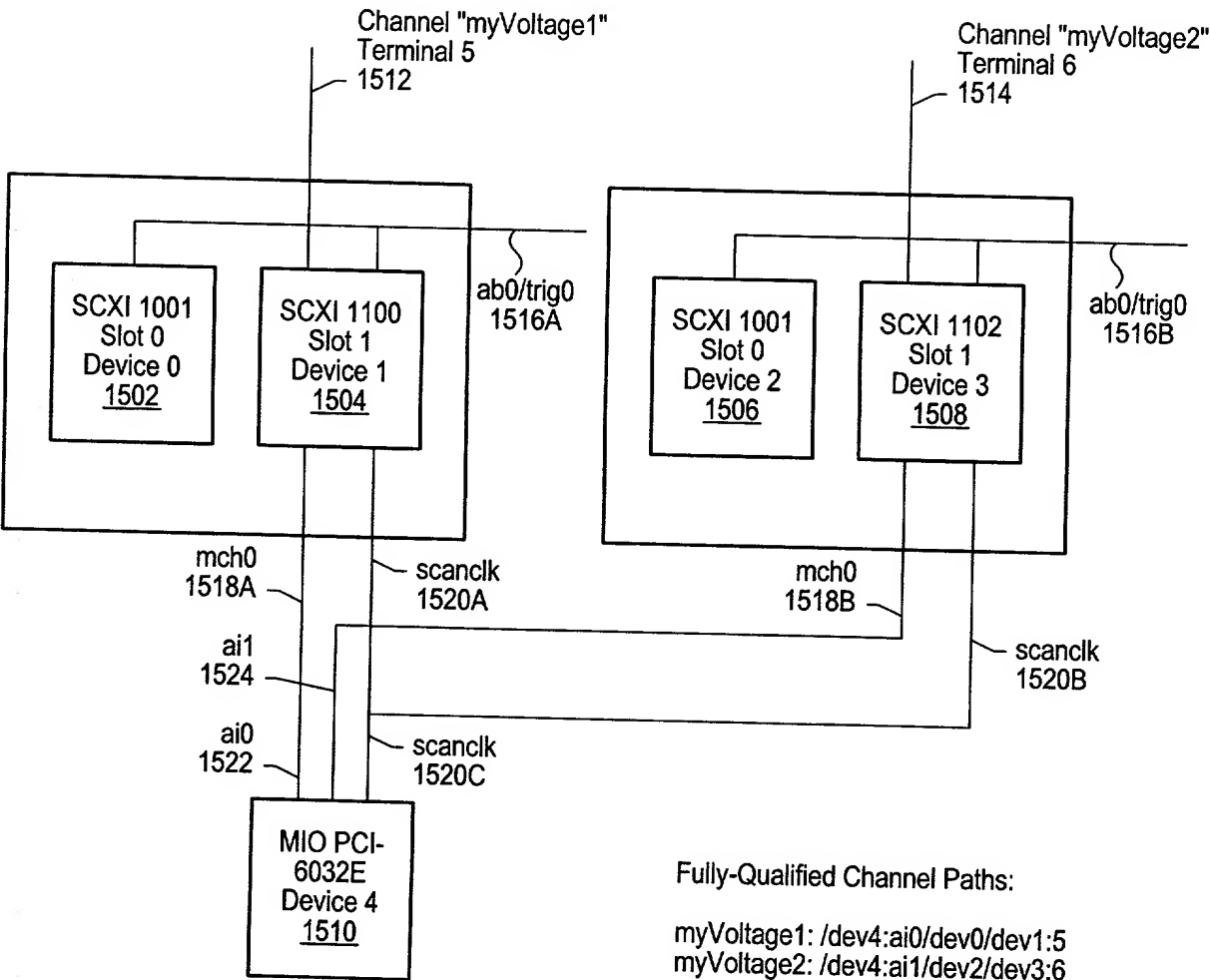


FIG. 15

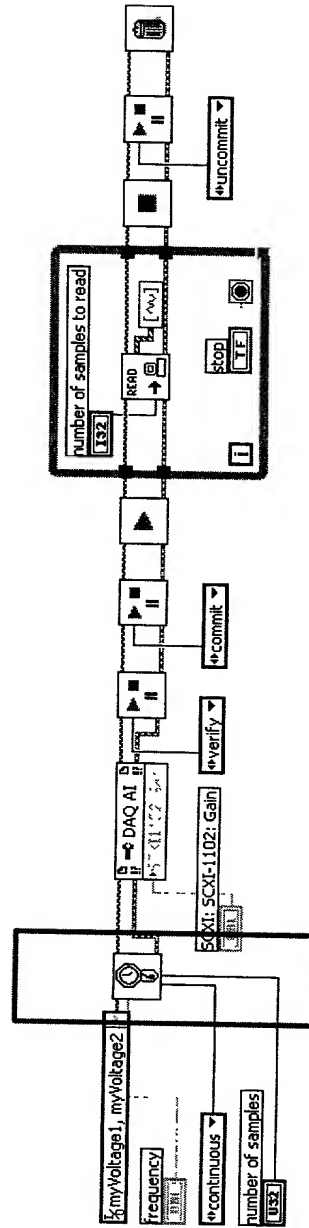
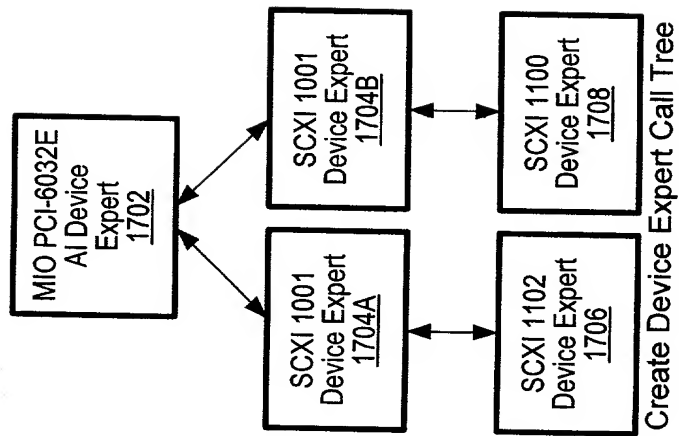
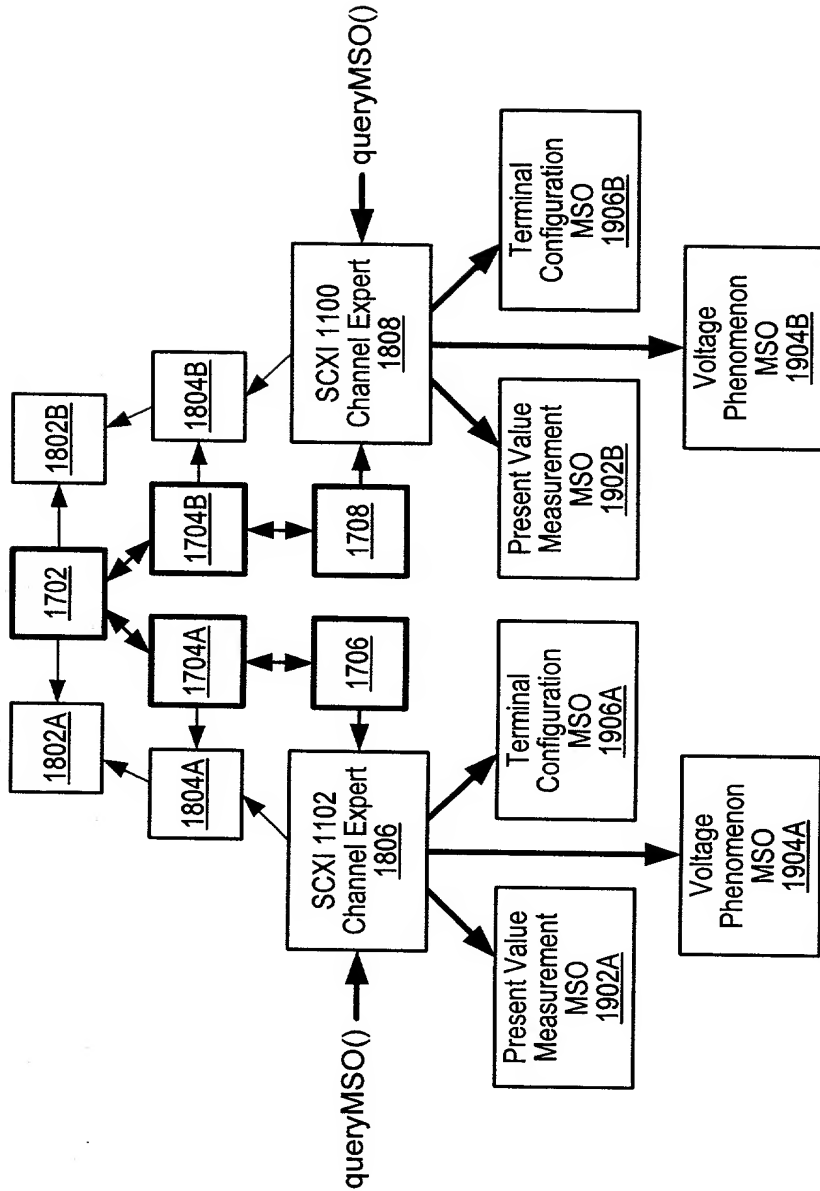


FIG. 17



Deserialize Named Channel MSOs

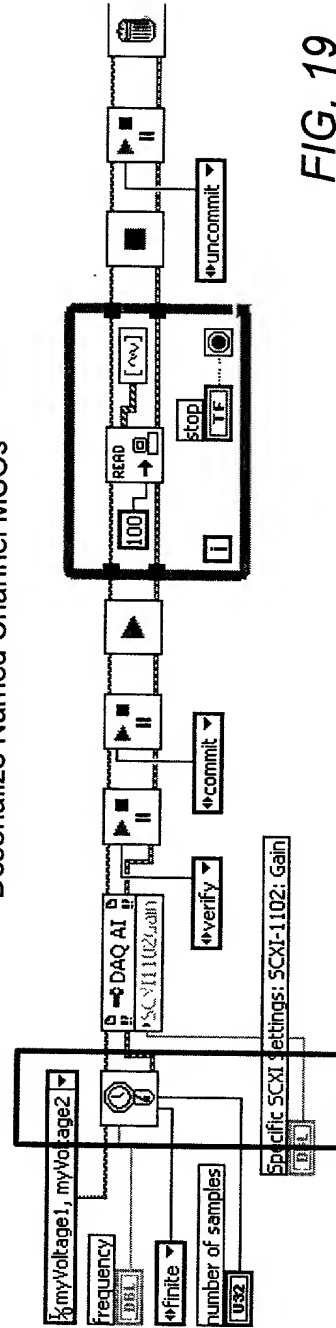


FIG. 19

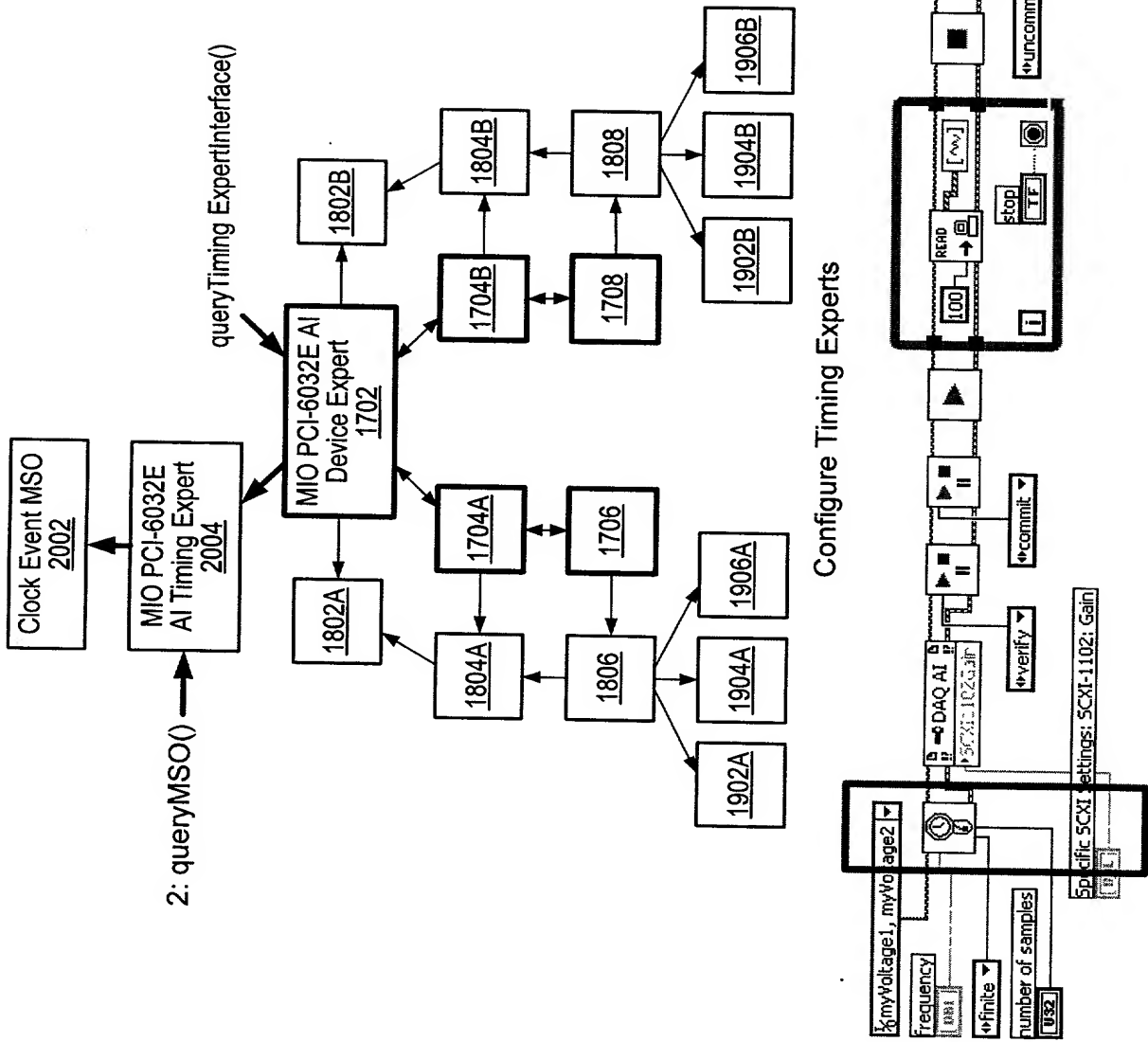


FIG. 20

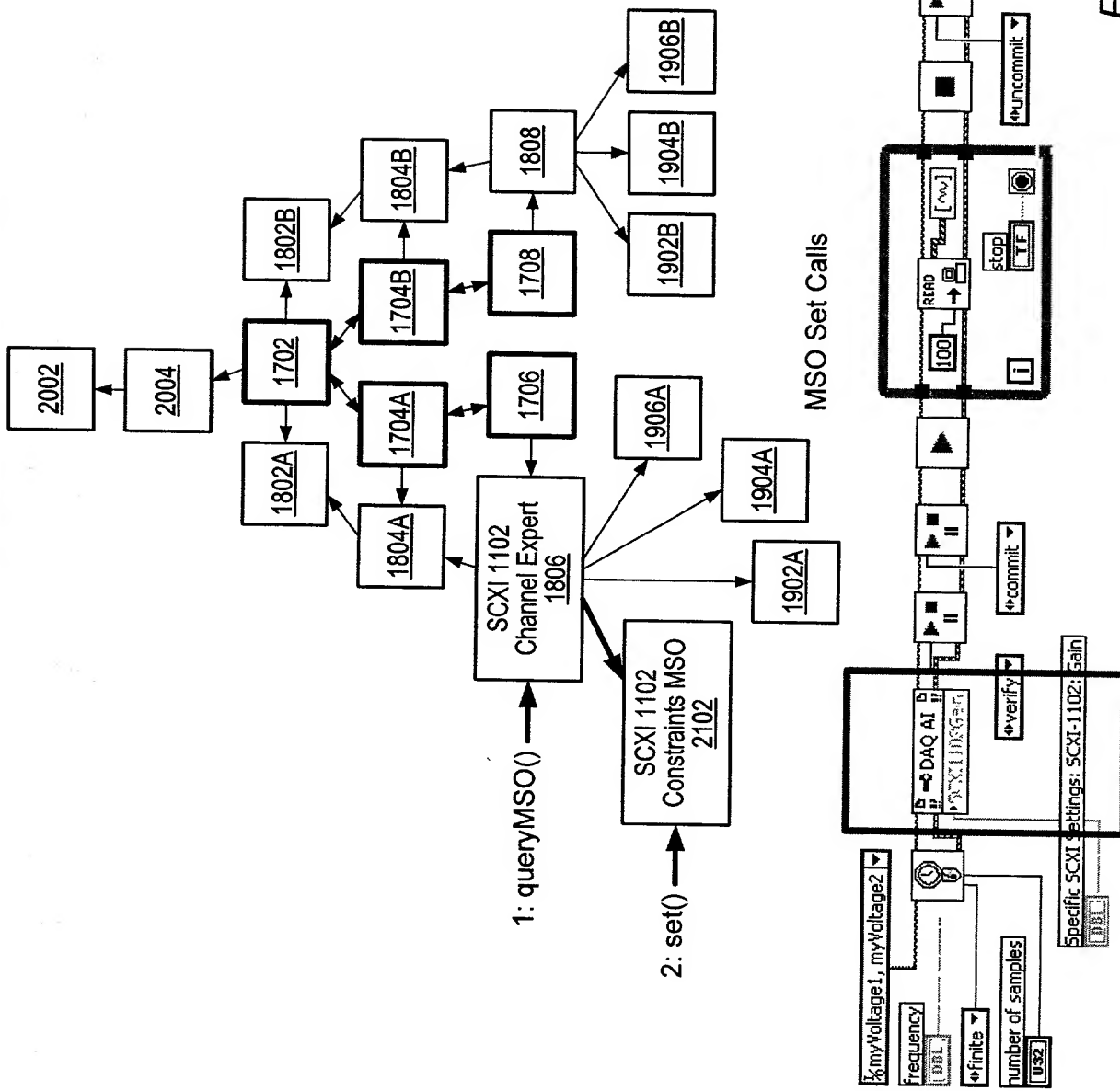
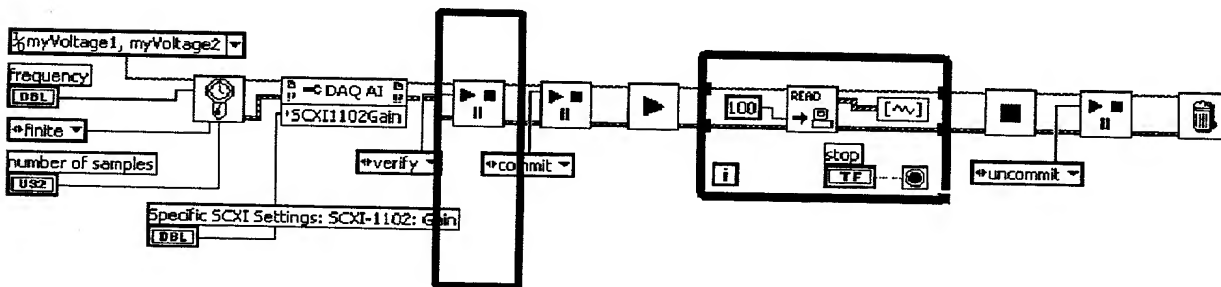
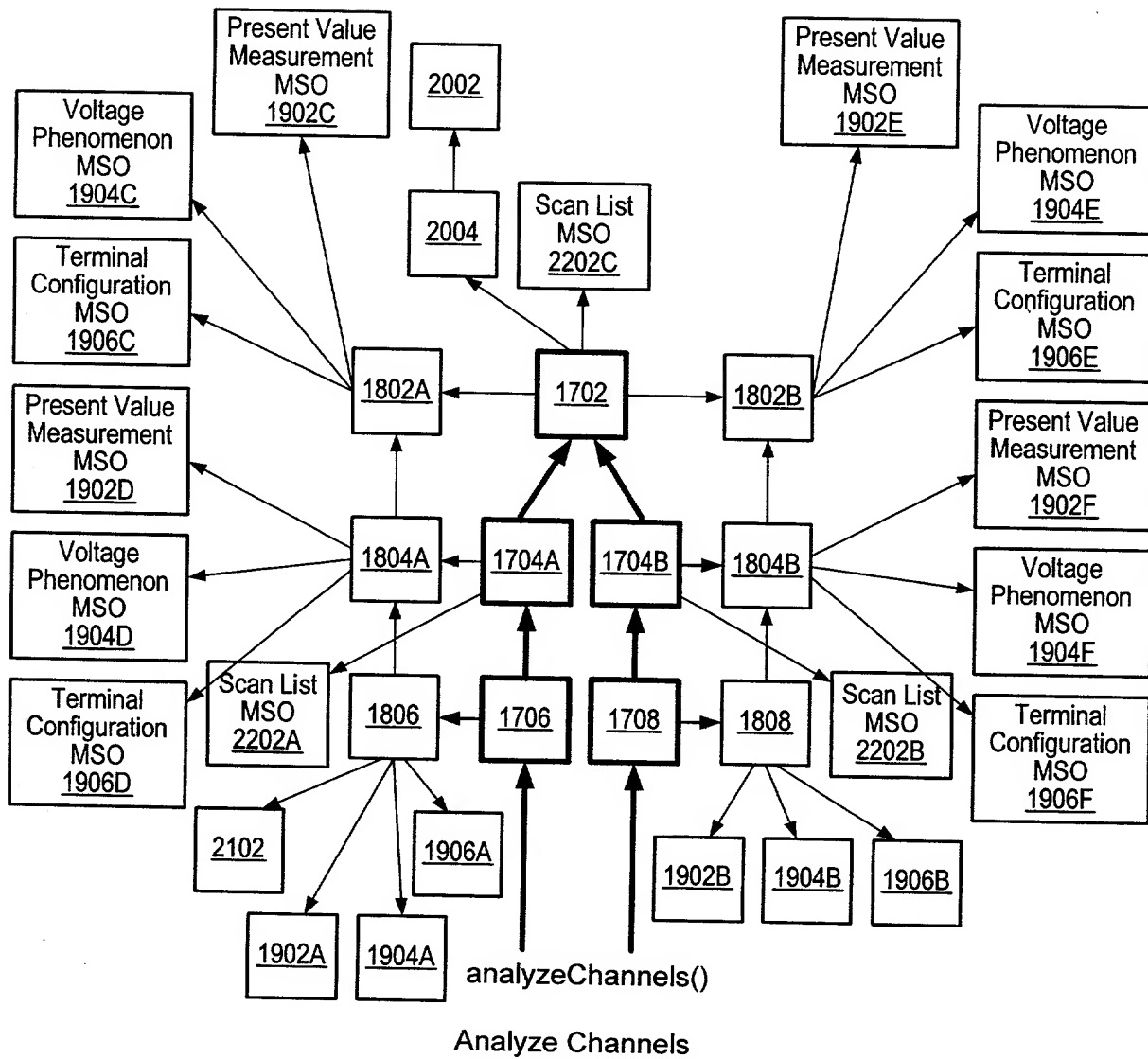
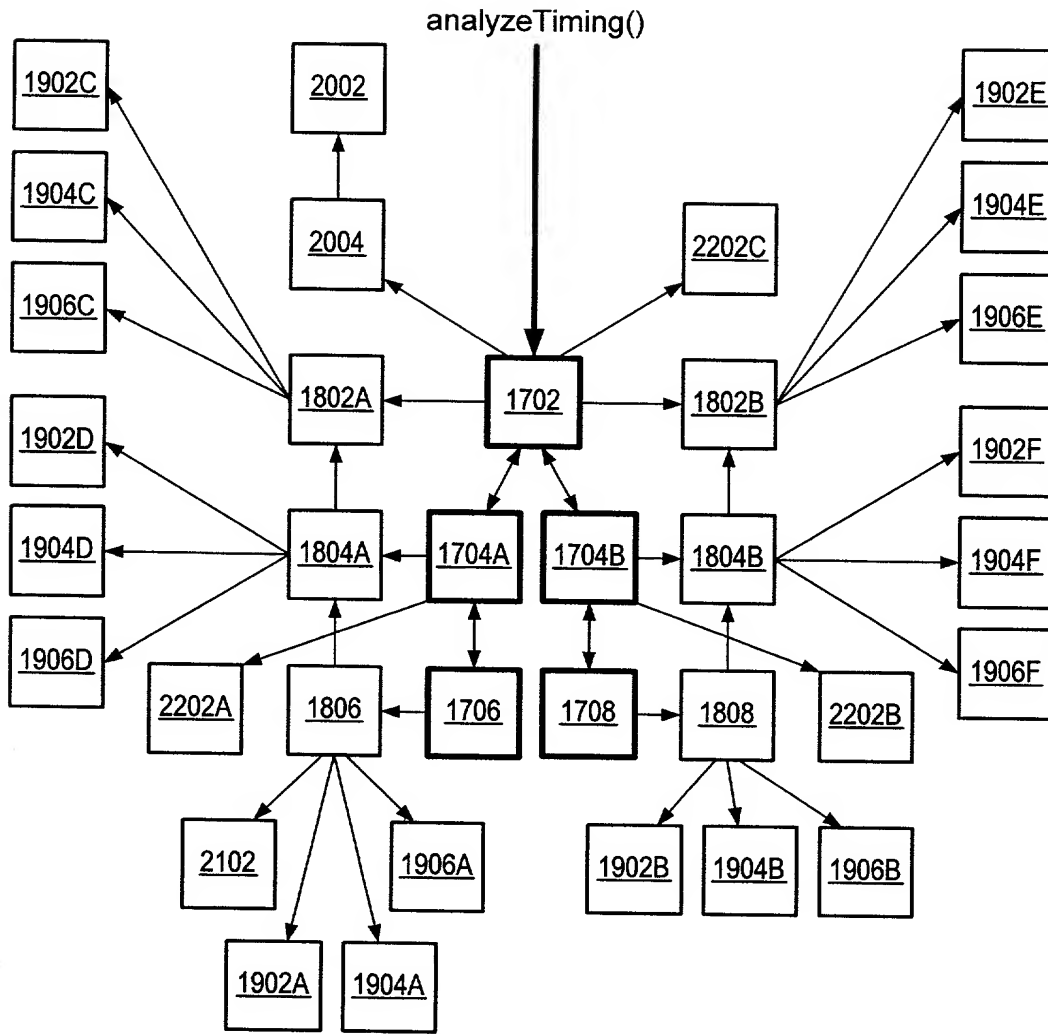


FIG. 21





Analyze Timing

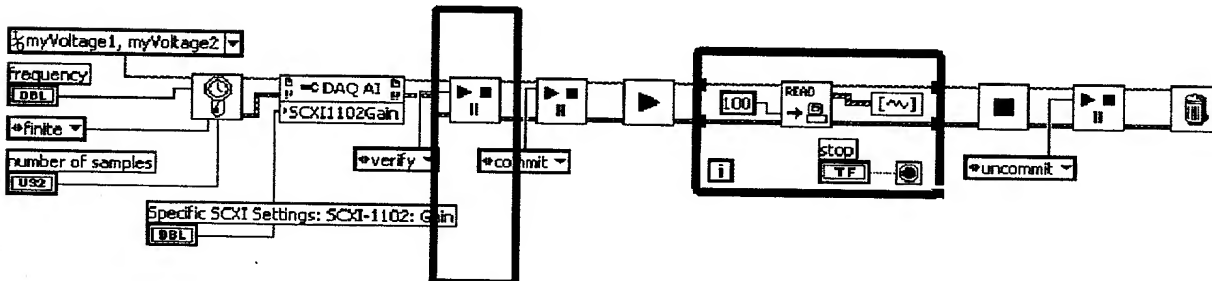


FIG. 23

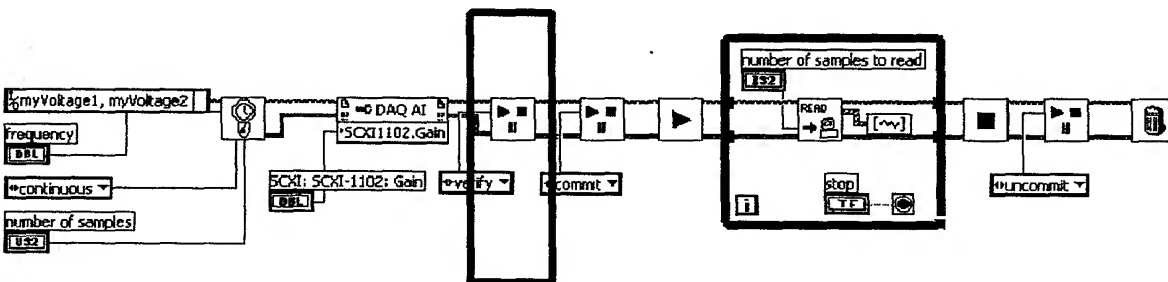
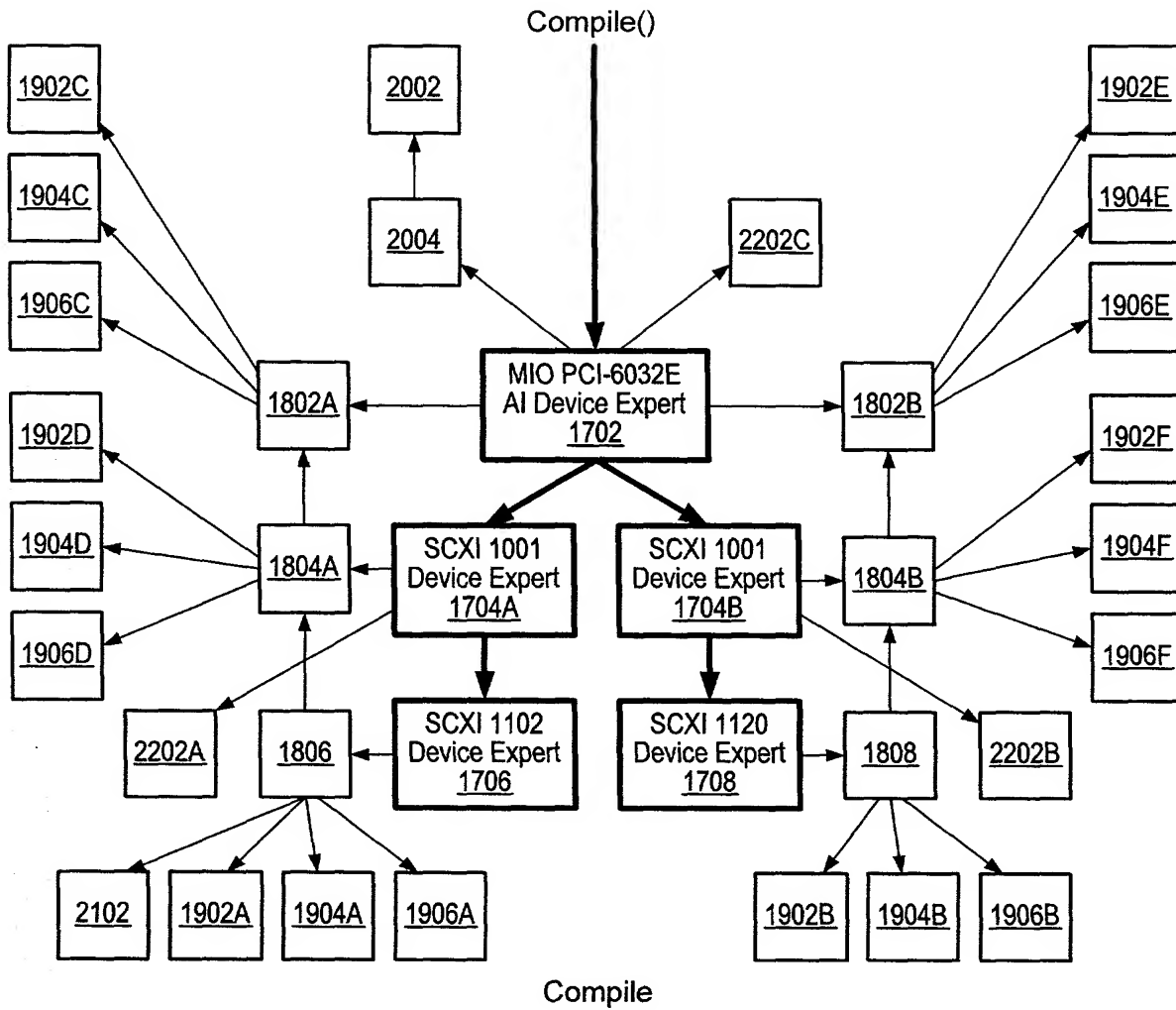


FIG. 24A

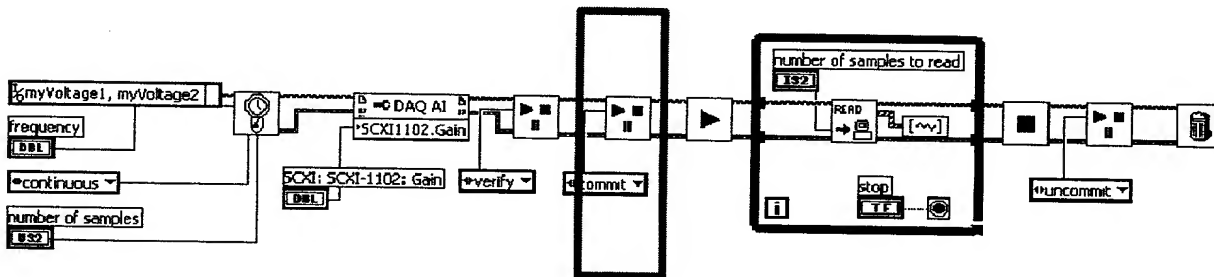
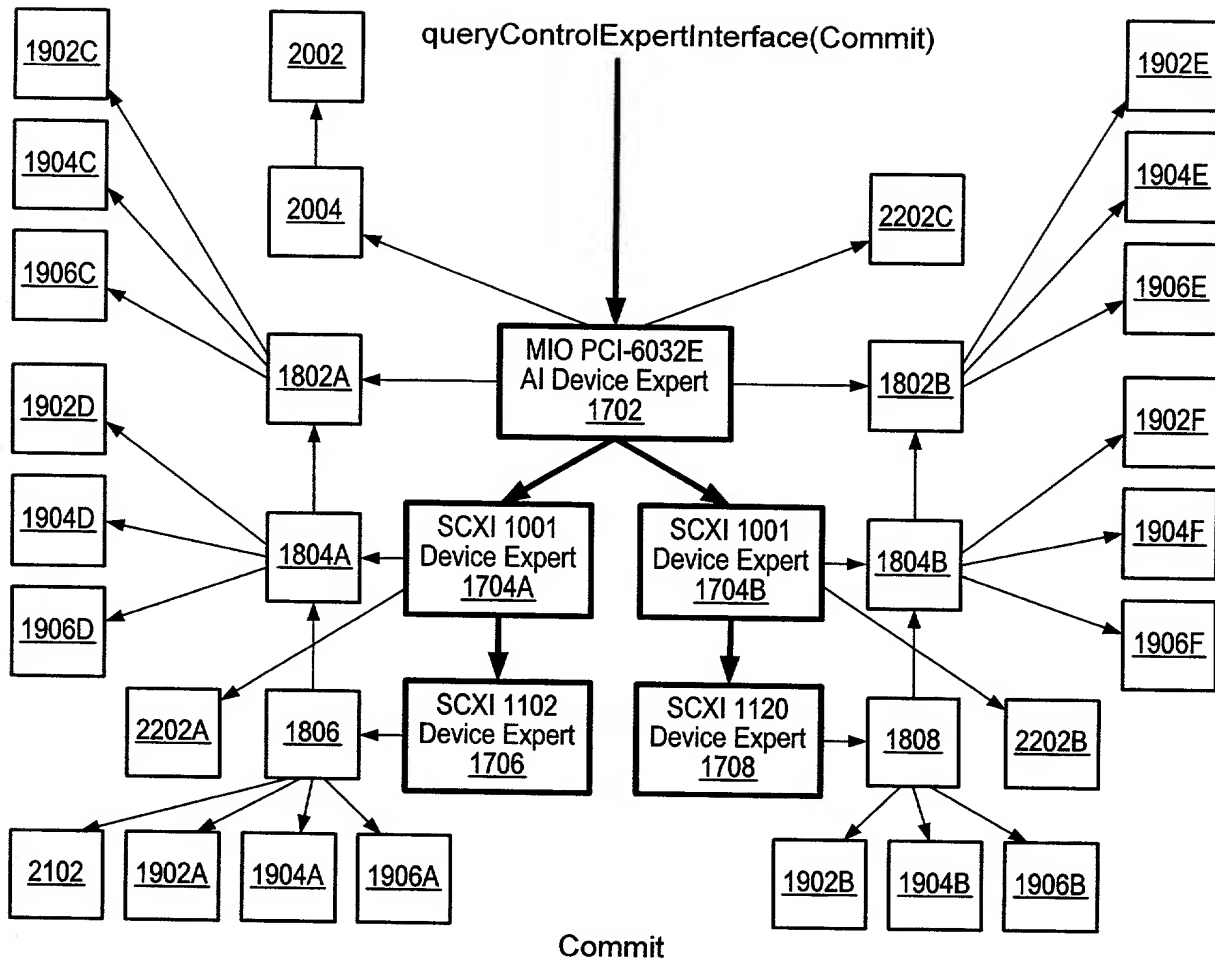


FIG. 24B

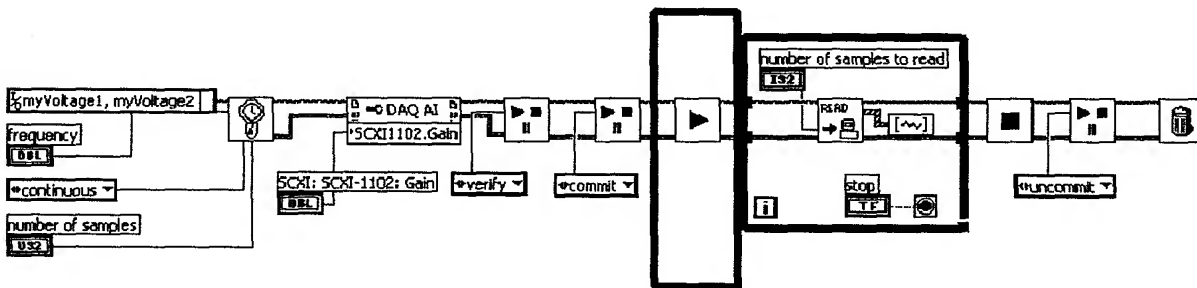
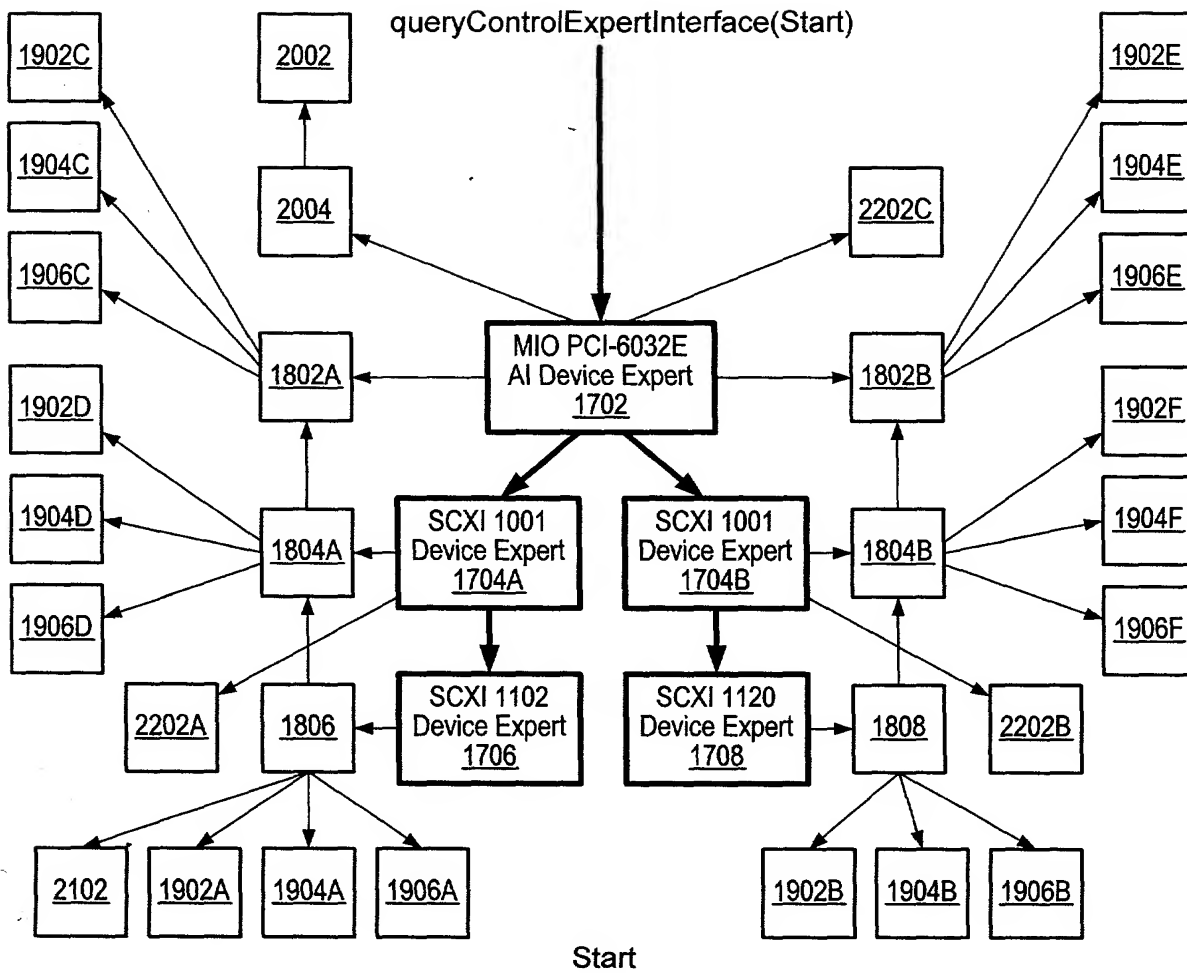


FIG. 24C

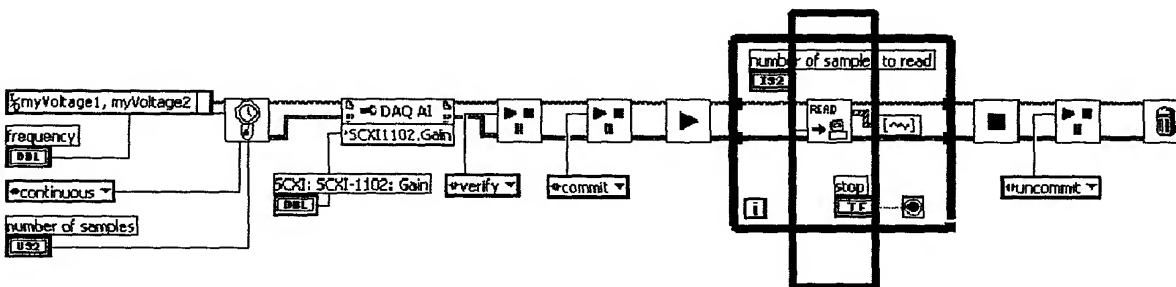
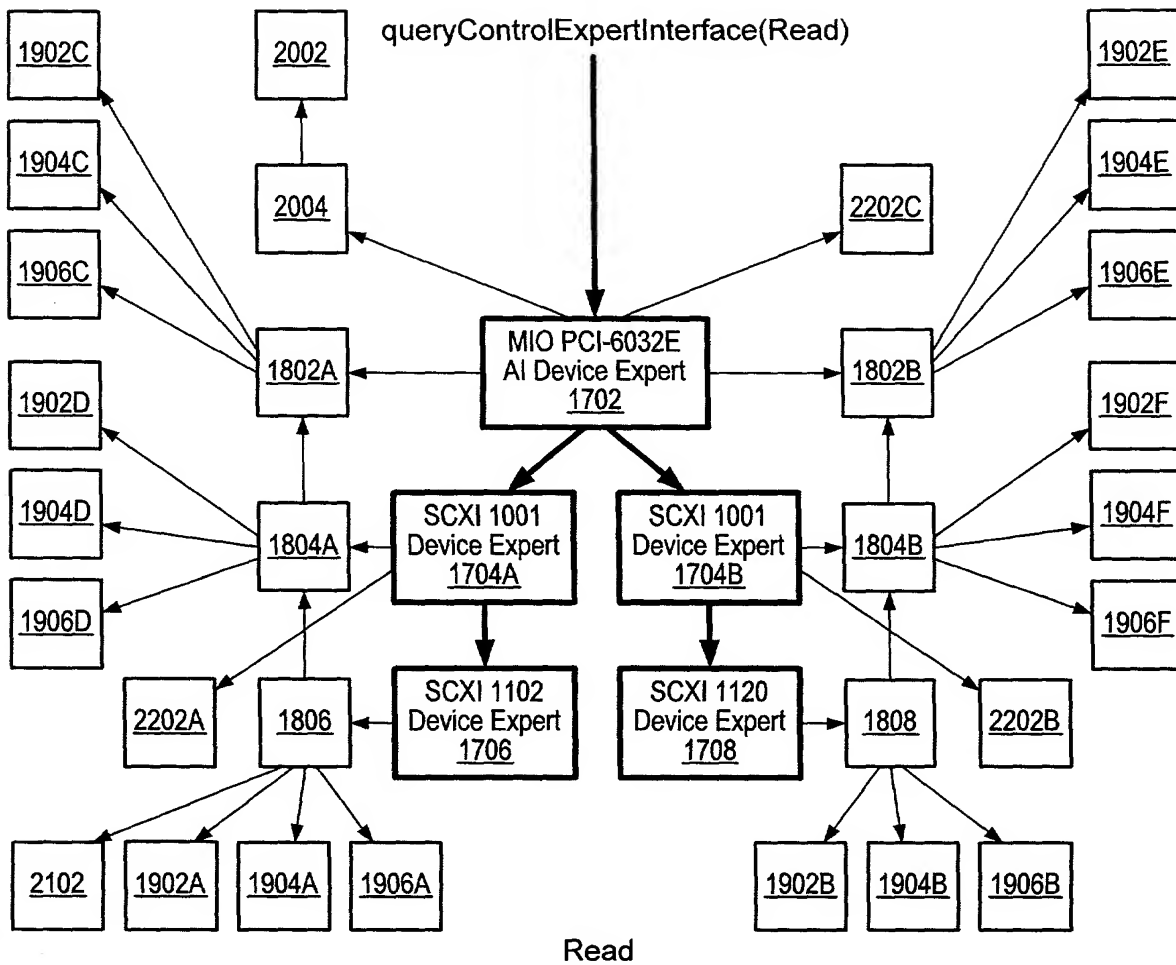


FIG. 24D

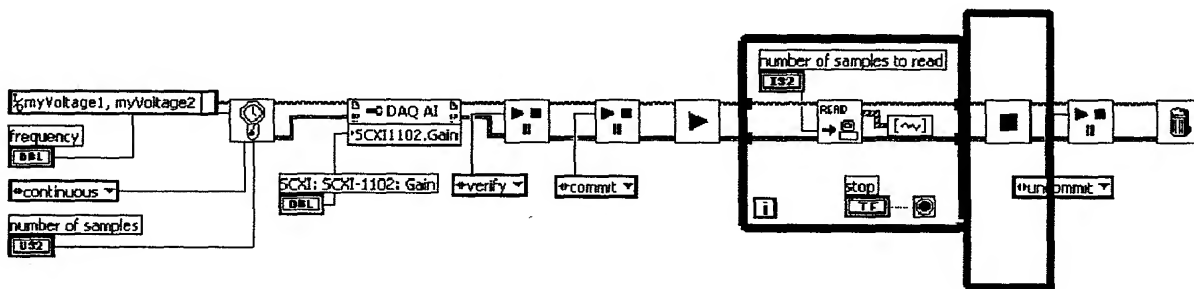
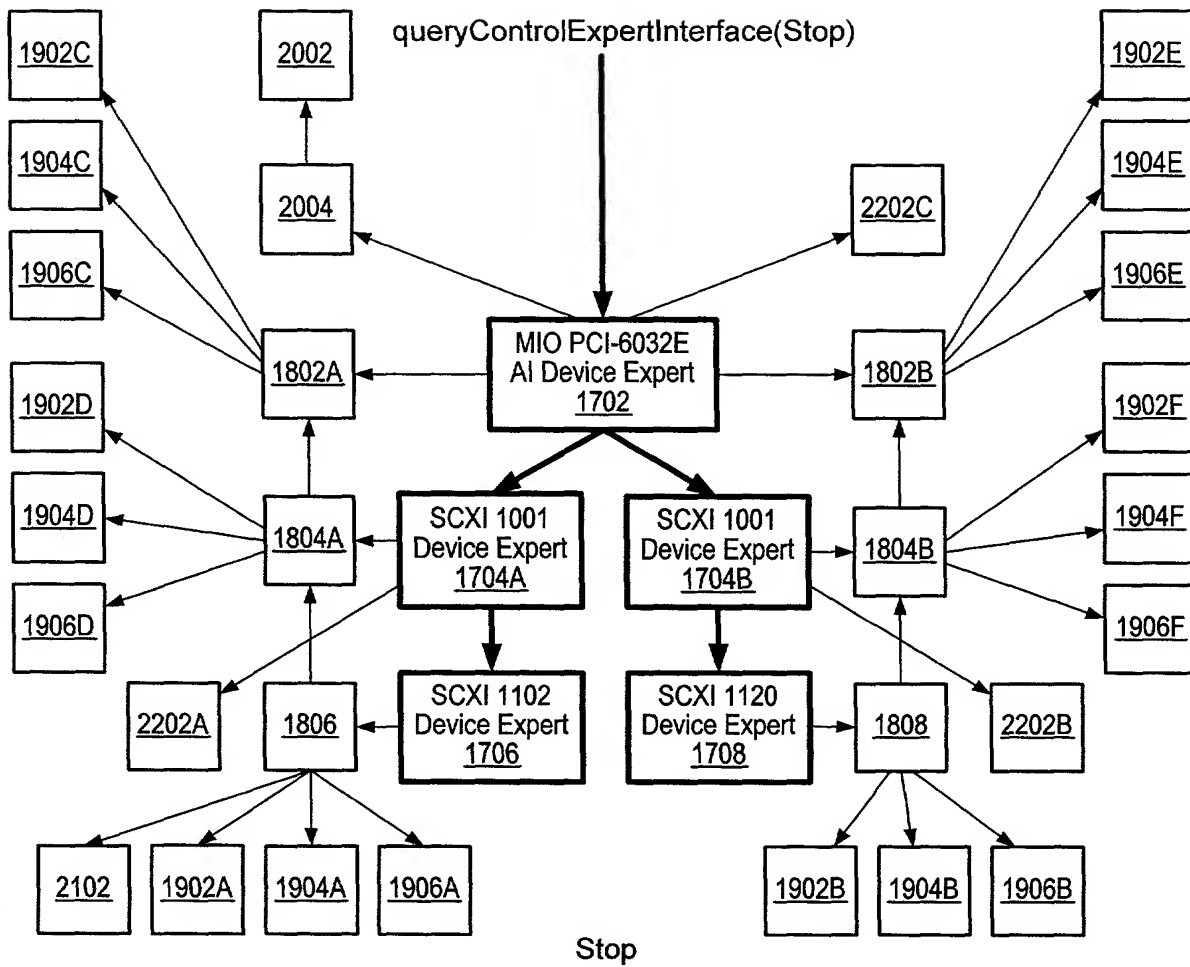


FIG. 24E

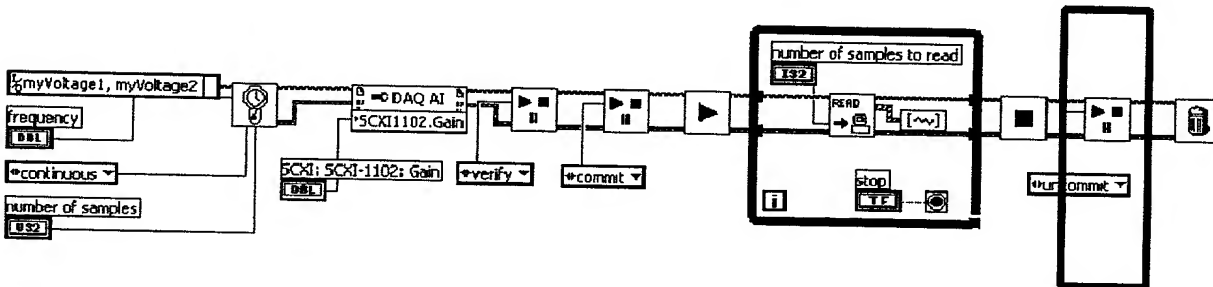
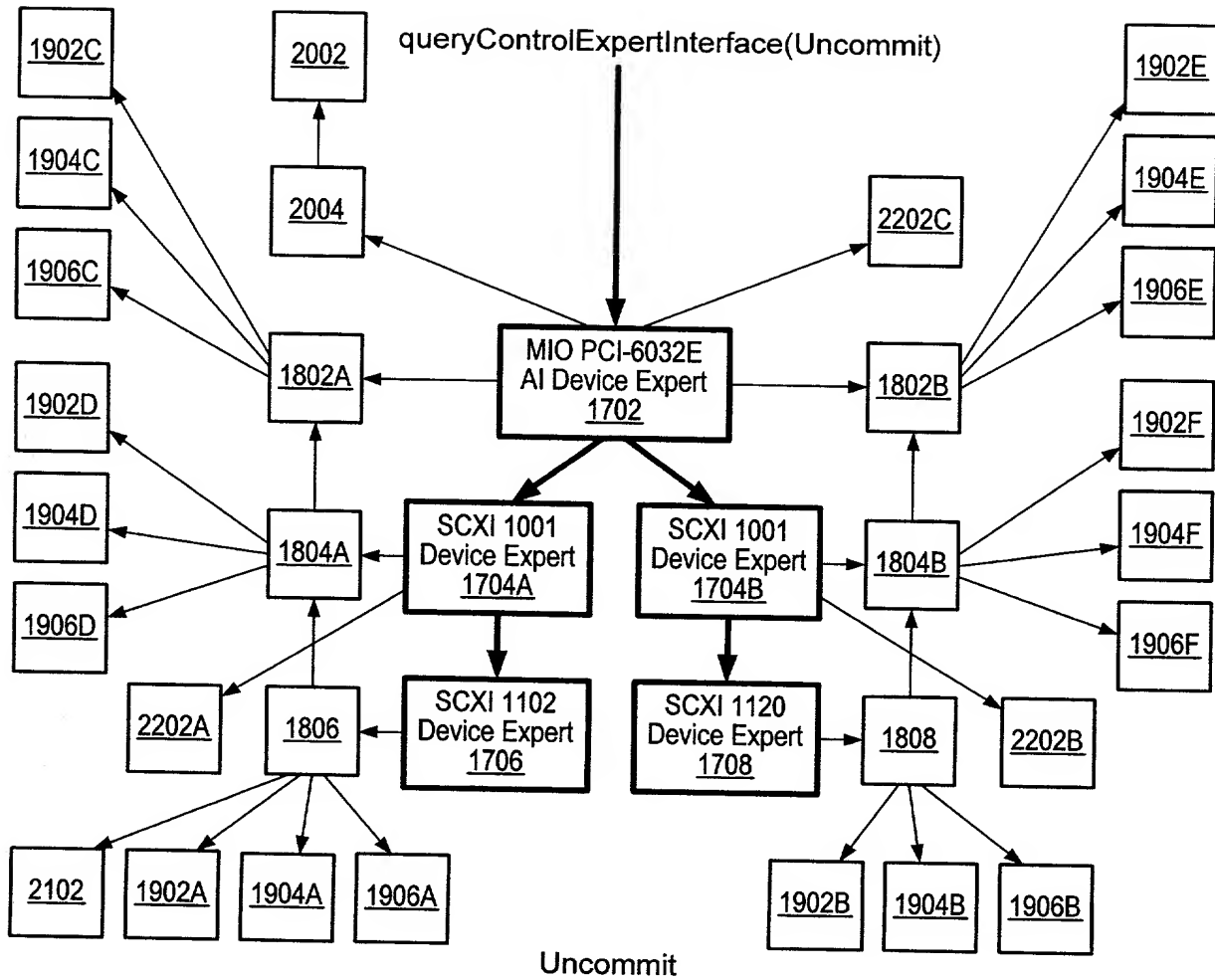
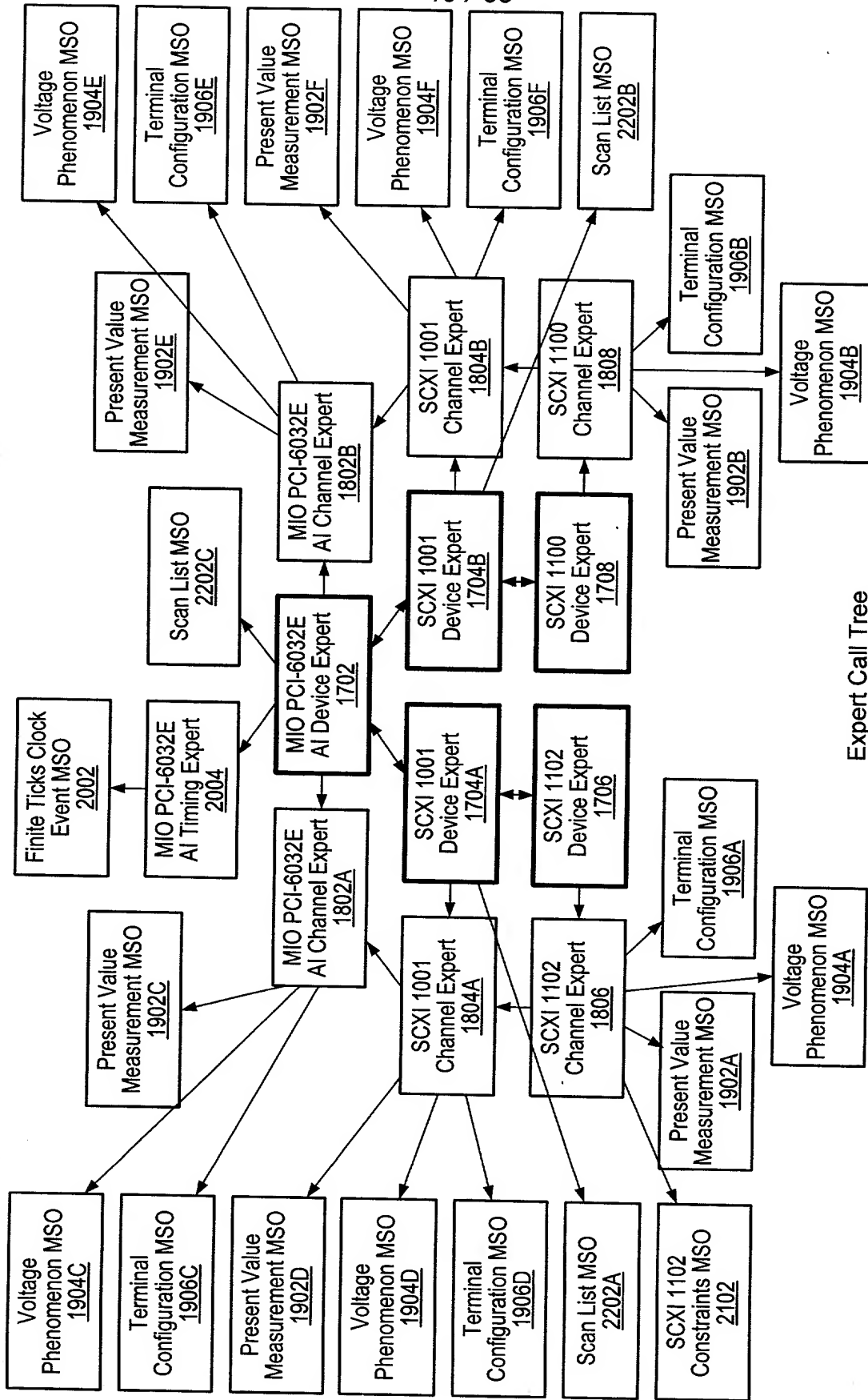


FIG. 24F



Expert Call Tree

Use Case: Multi-Chassis SCXI Finite Acquisition Using An MIO

FIG. 25

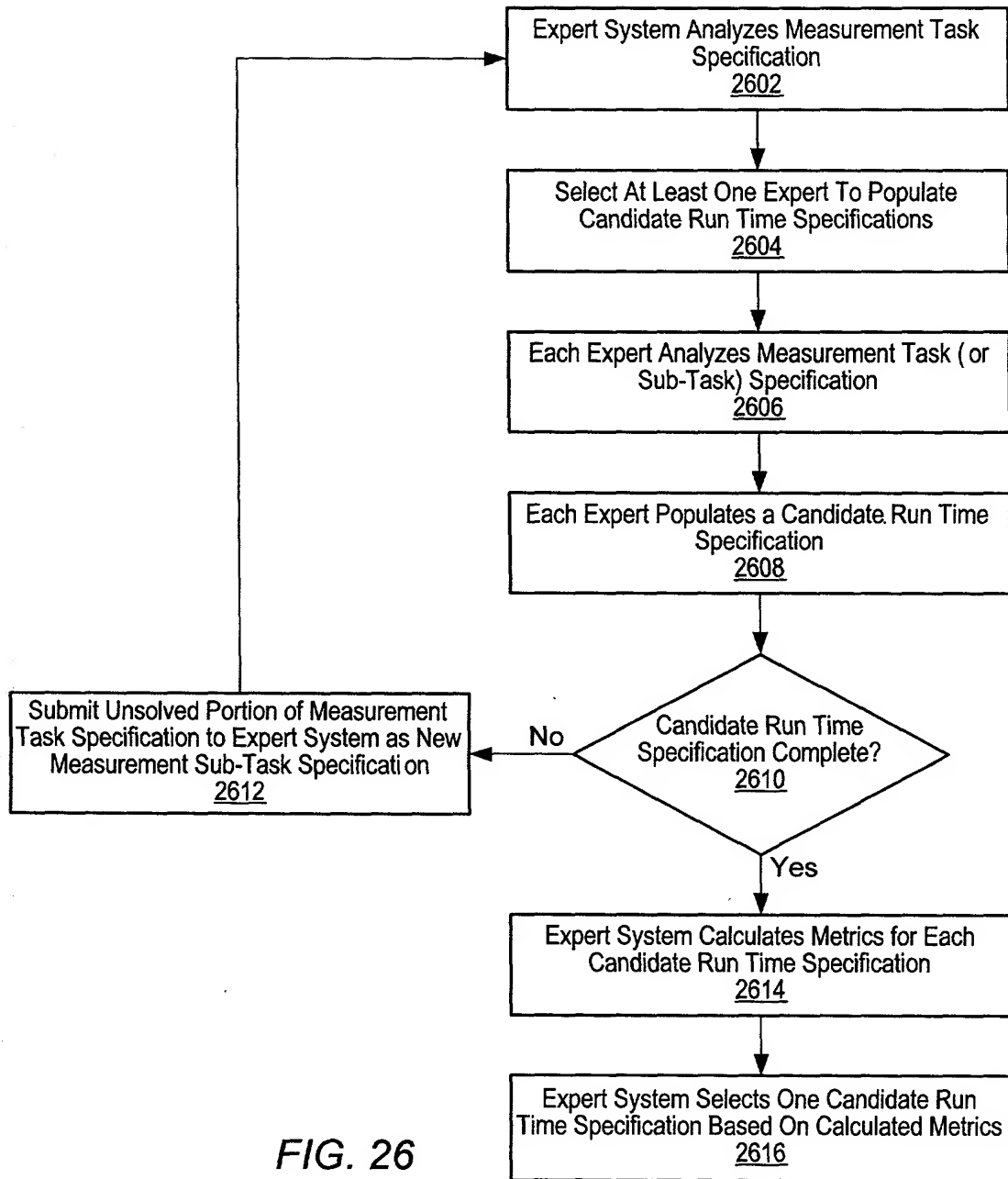


FIG. 26

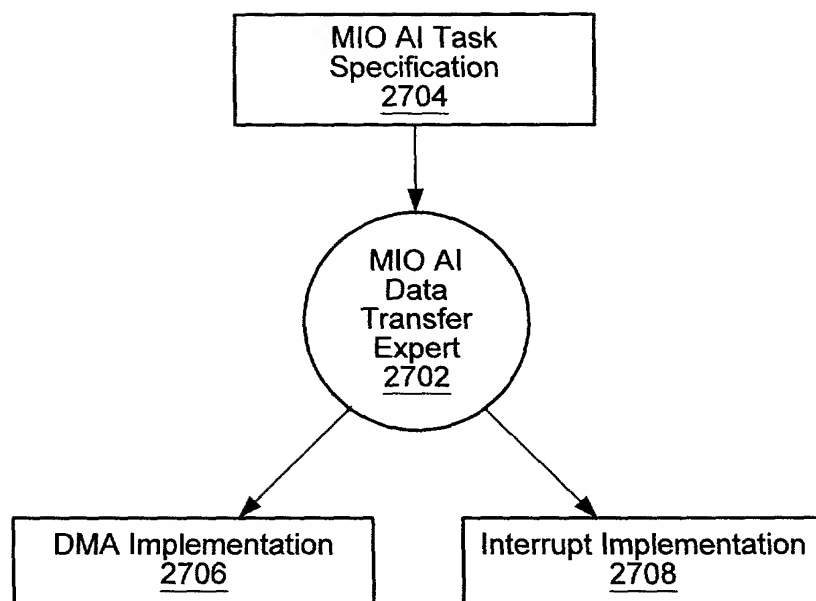


FIG. 27

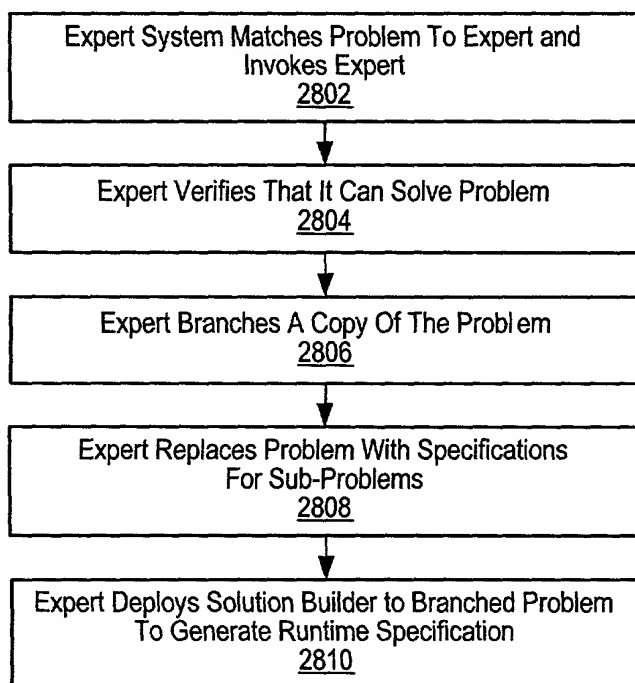


FIG. 28

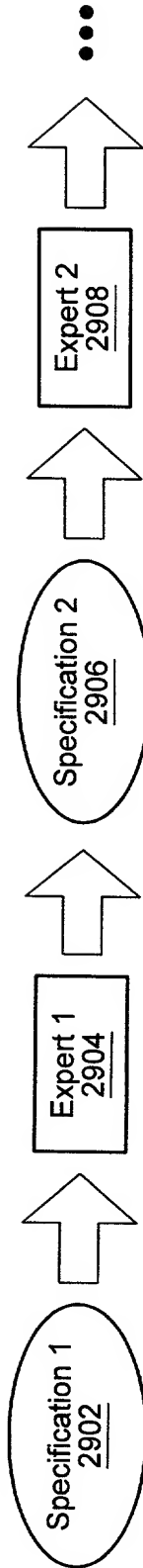


FIG. 29

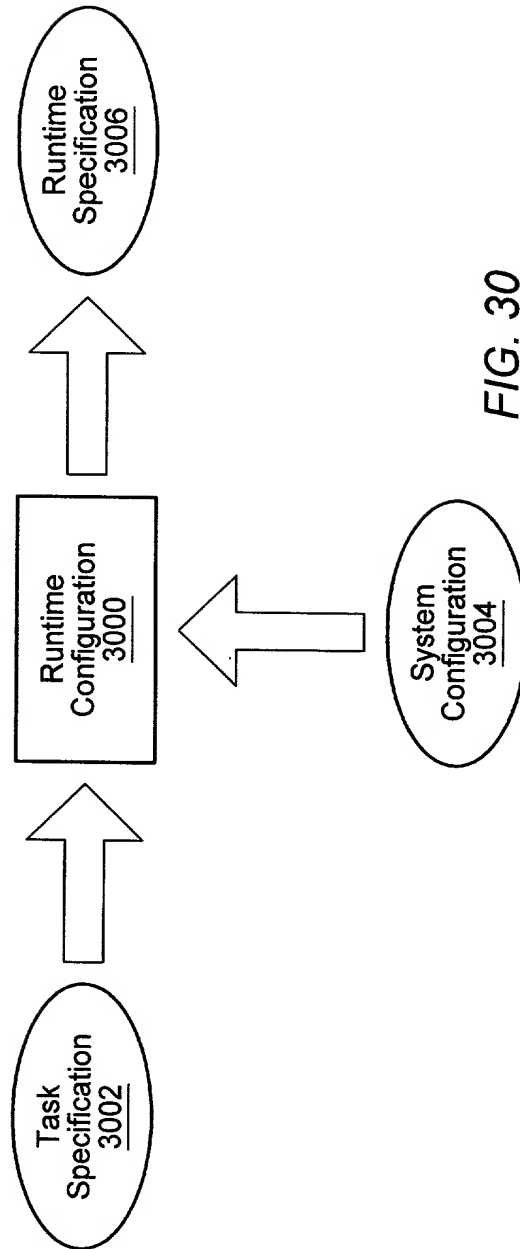


FIG. 30

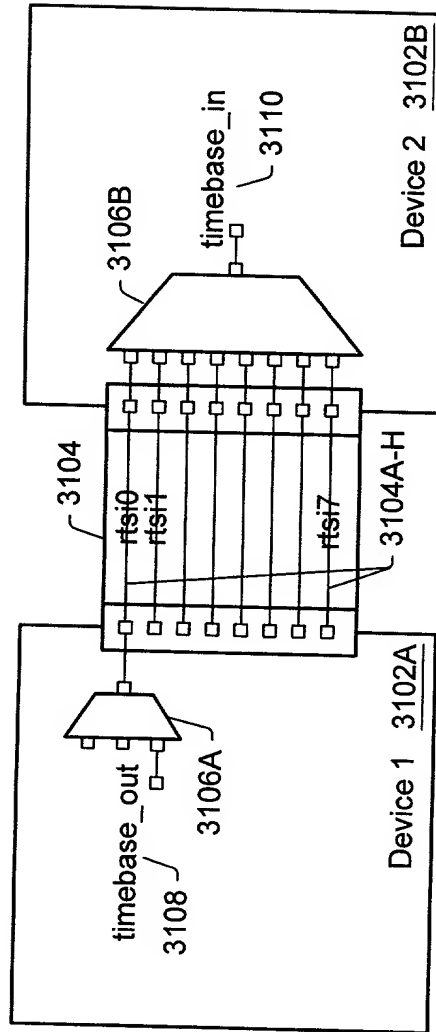


FIG. 31

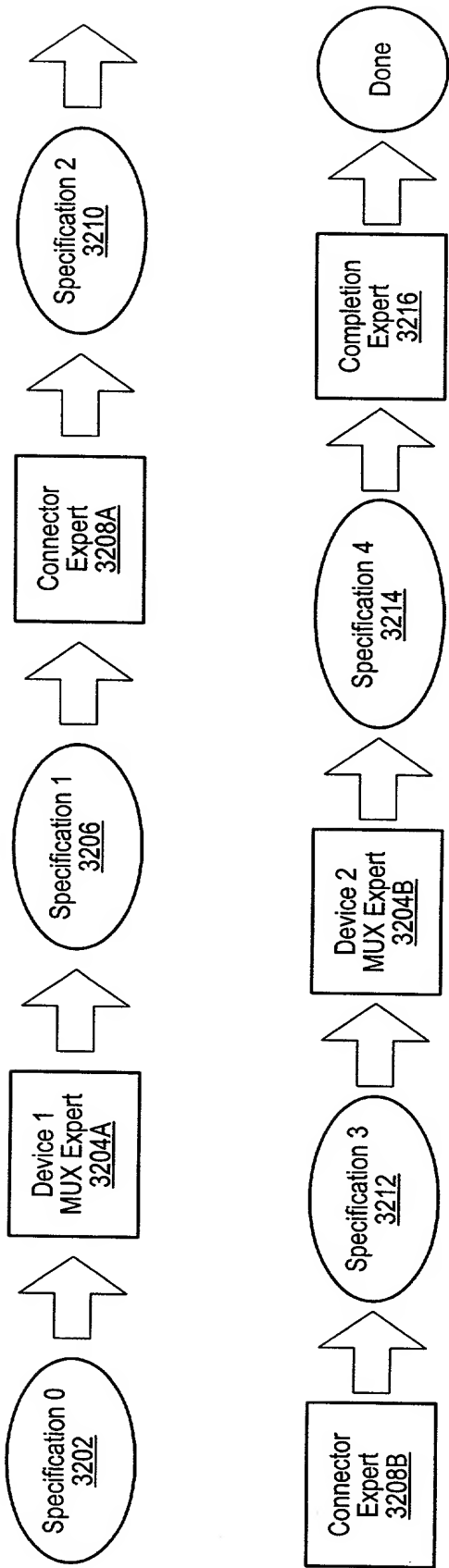


FIG. 32

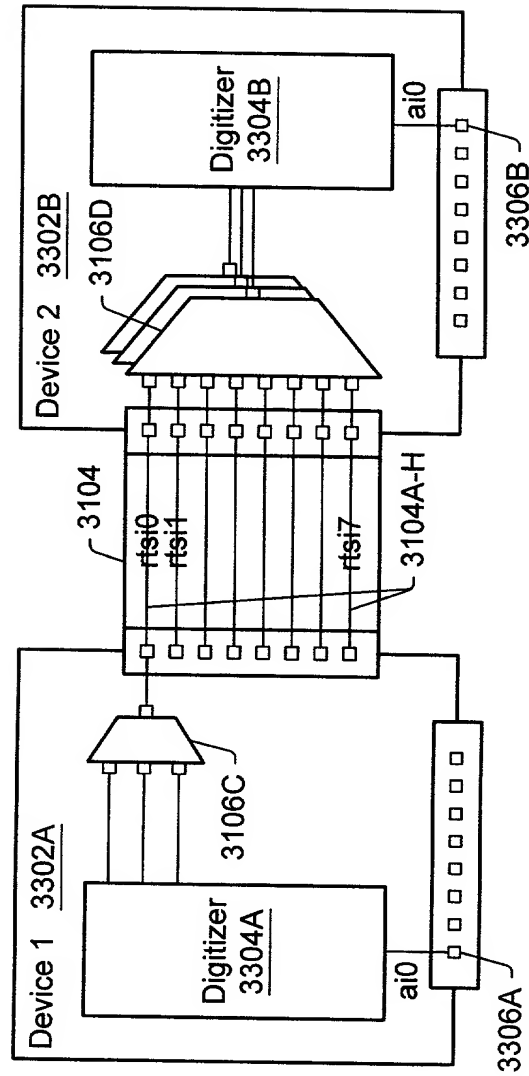


FIG. 33

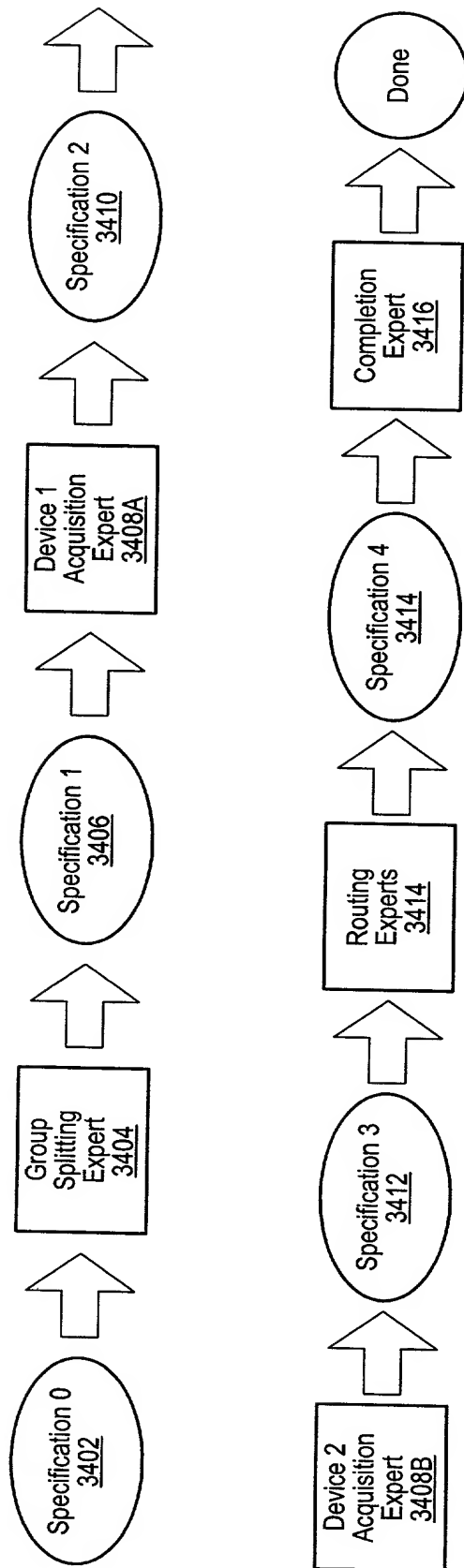


FIG. 34

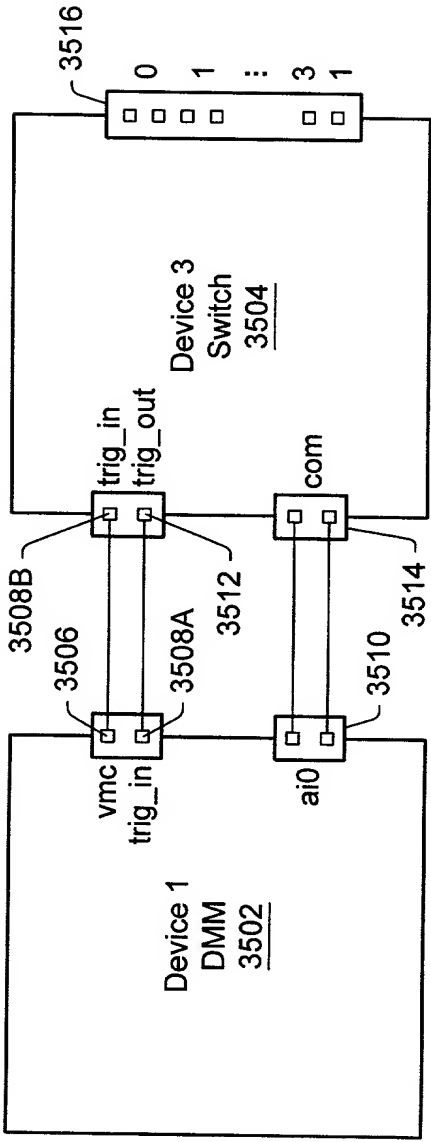


FIG. 35

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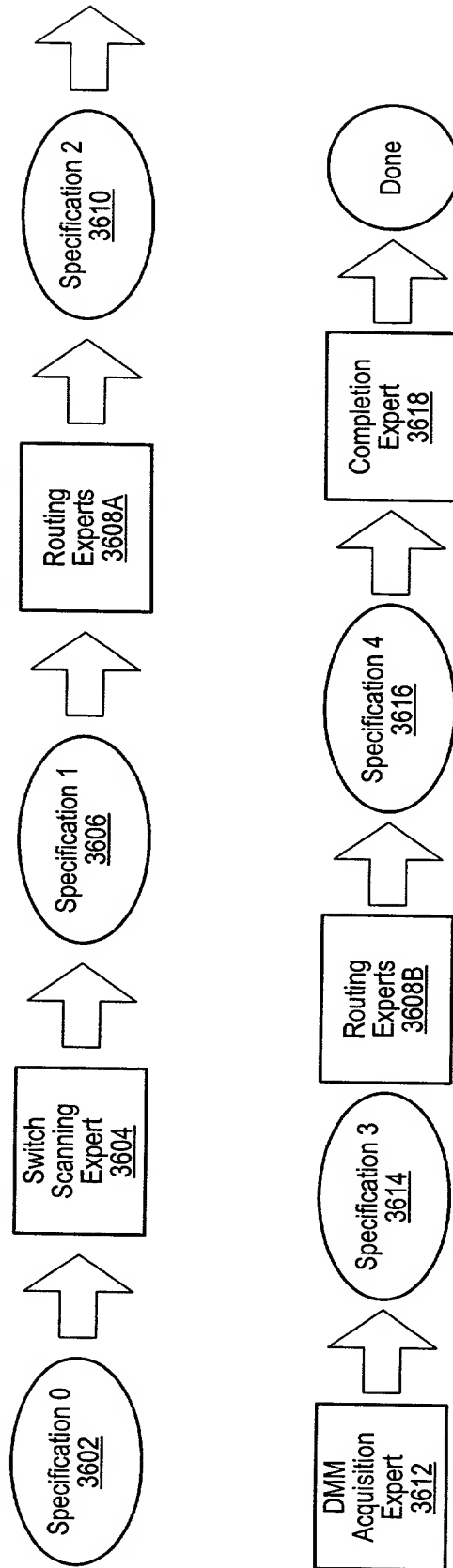
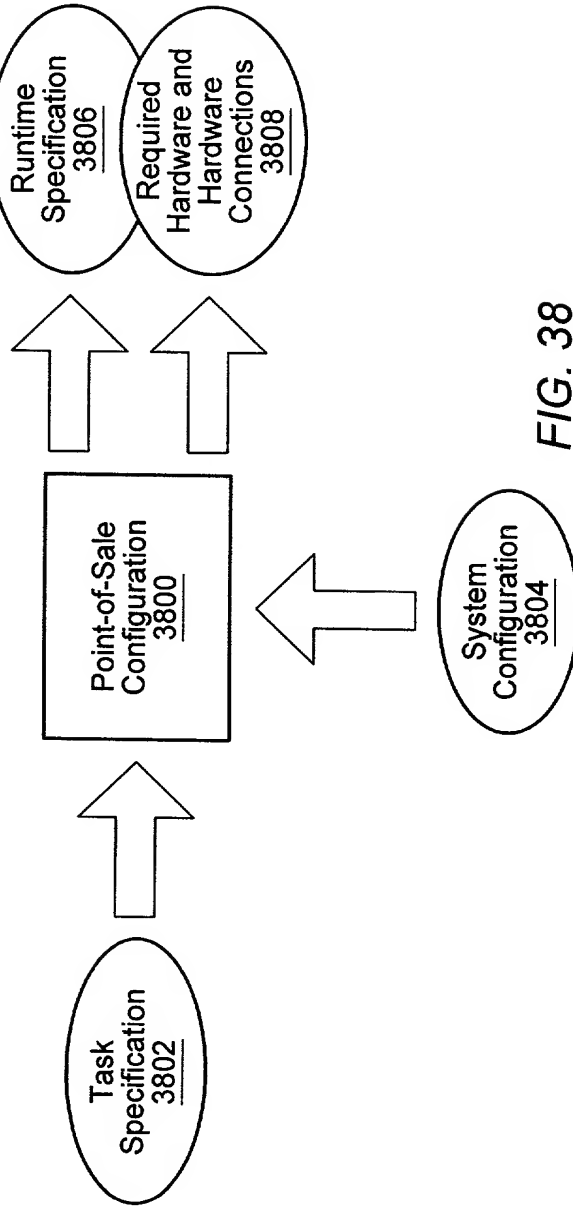
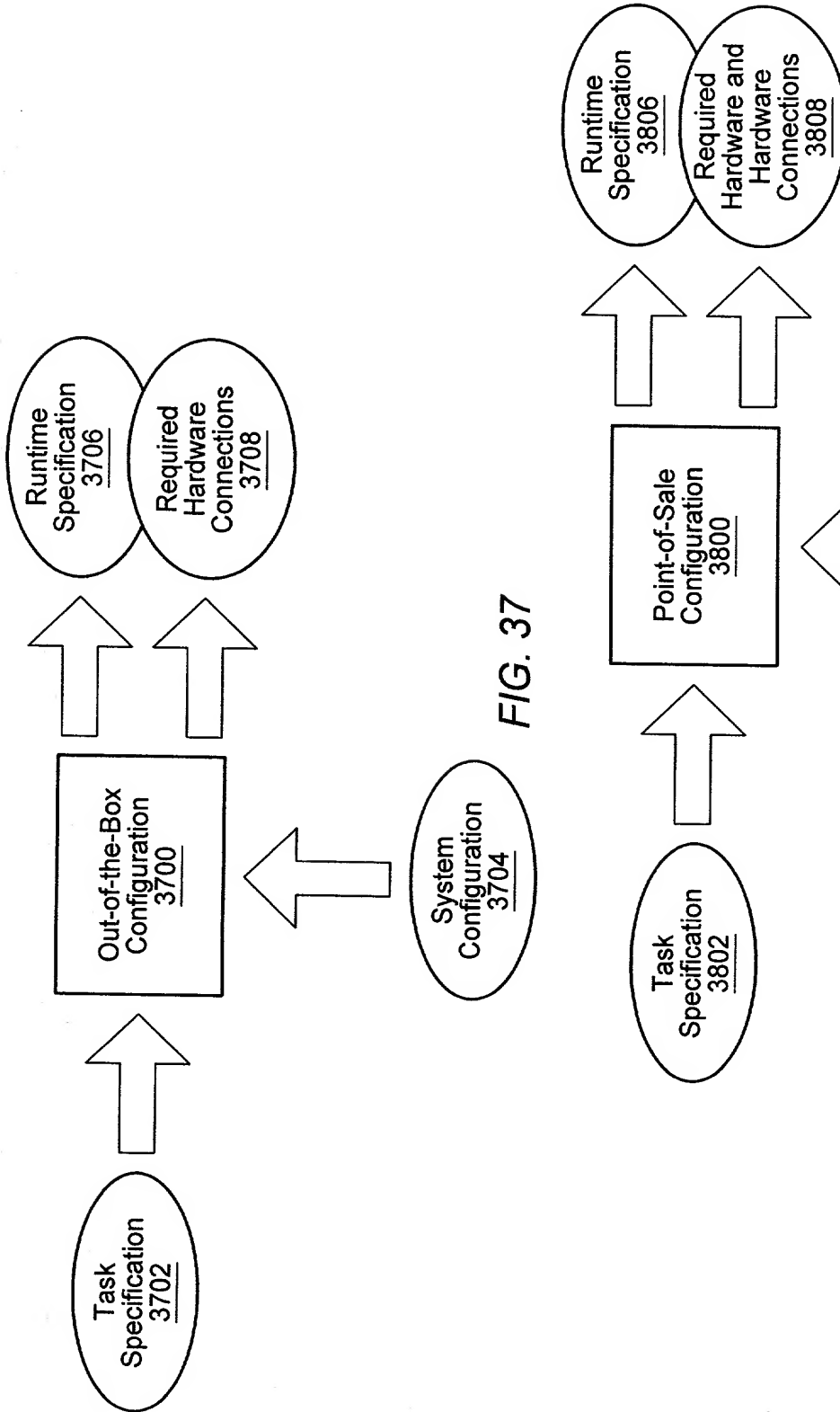
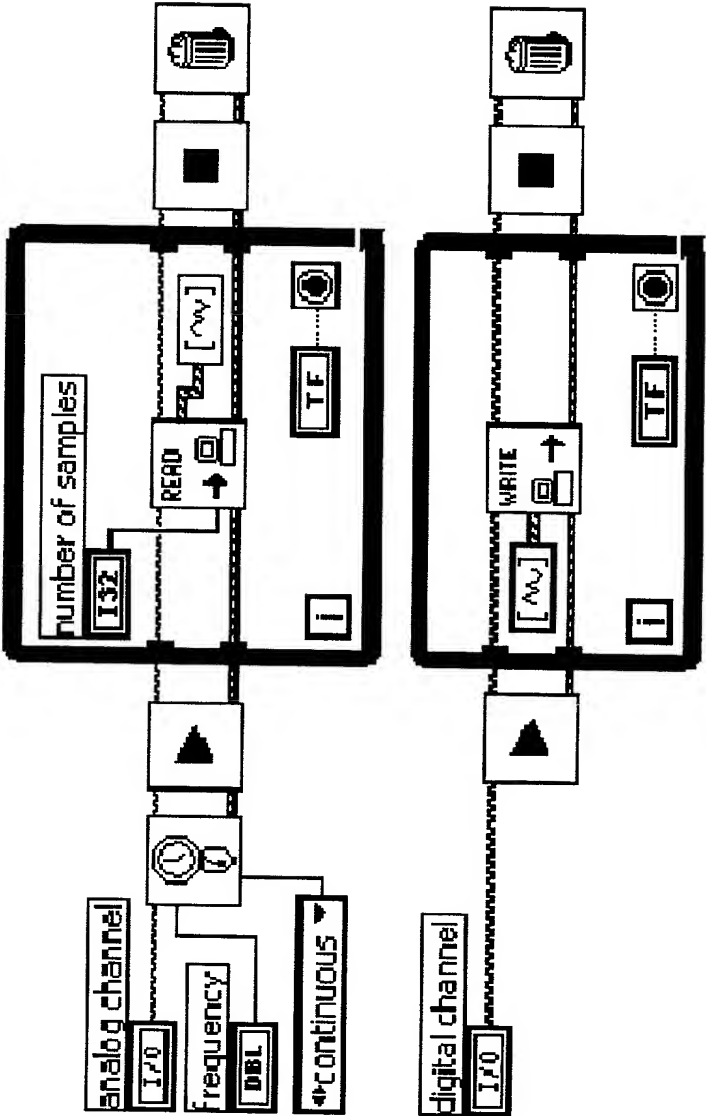


FIG. 36

208220" 262800T





Simultaneous Buffered Analog Input And Single Point
Digital Output With Multi-Threaded Driver

FIG. 39B

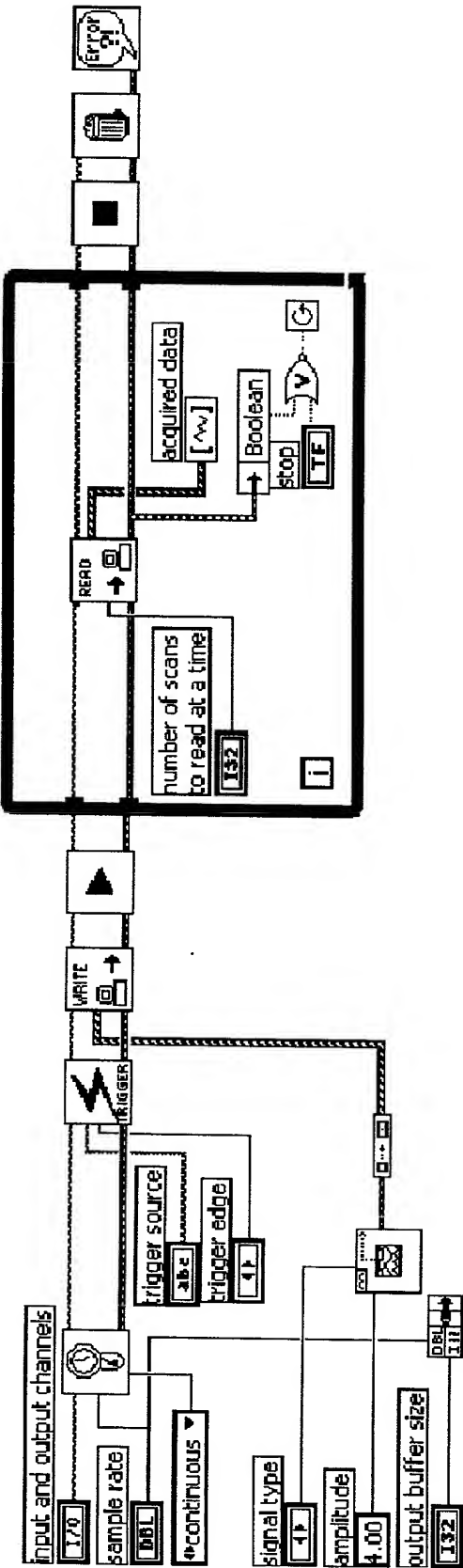
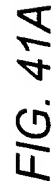
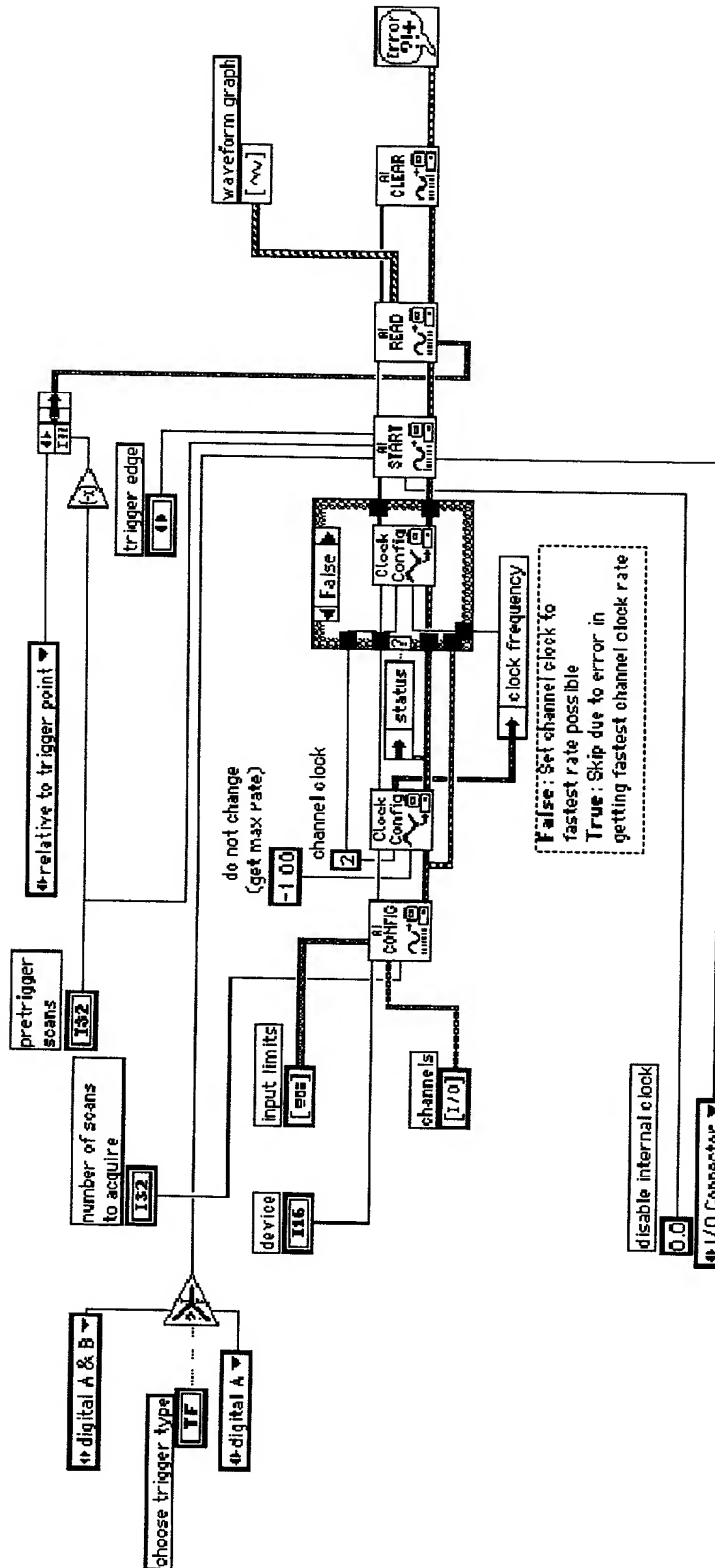


FIG. 40B

Simultaneous Triggered Buffered AII/O



Sharing Scan Clock Across Two E-Series Devices (Prior Art)



Acquire N Scans External Scan Clock Digital Trigger (Prior Art)

FIG. 43A
(Prior Art)

208220" 2648000T

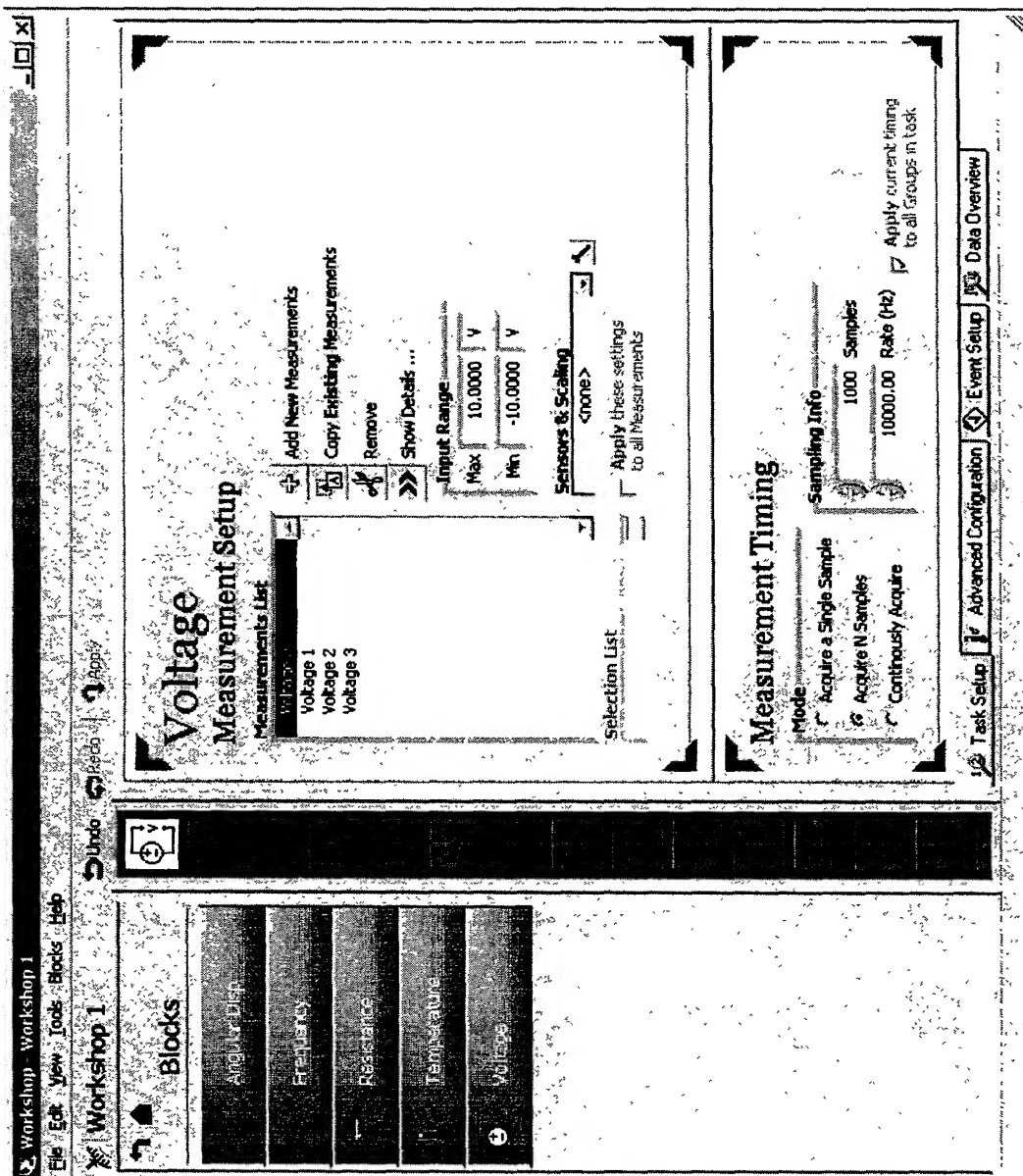


FIG. 43B

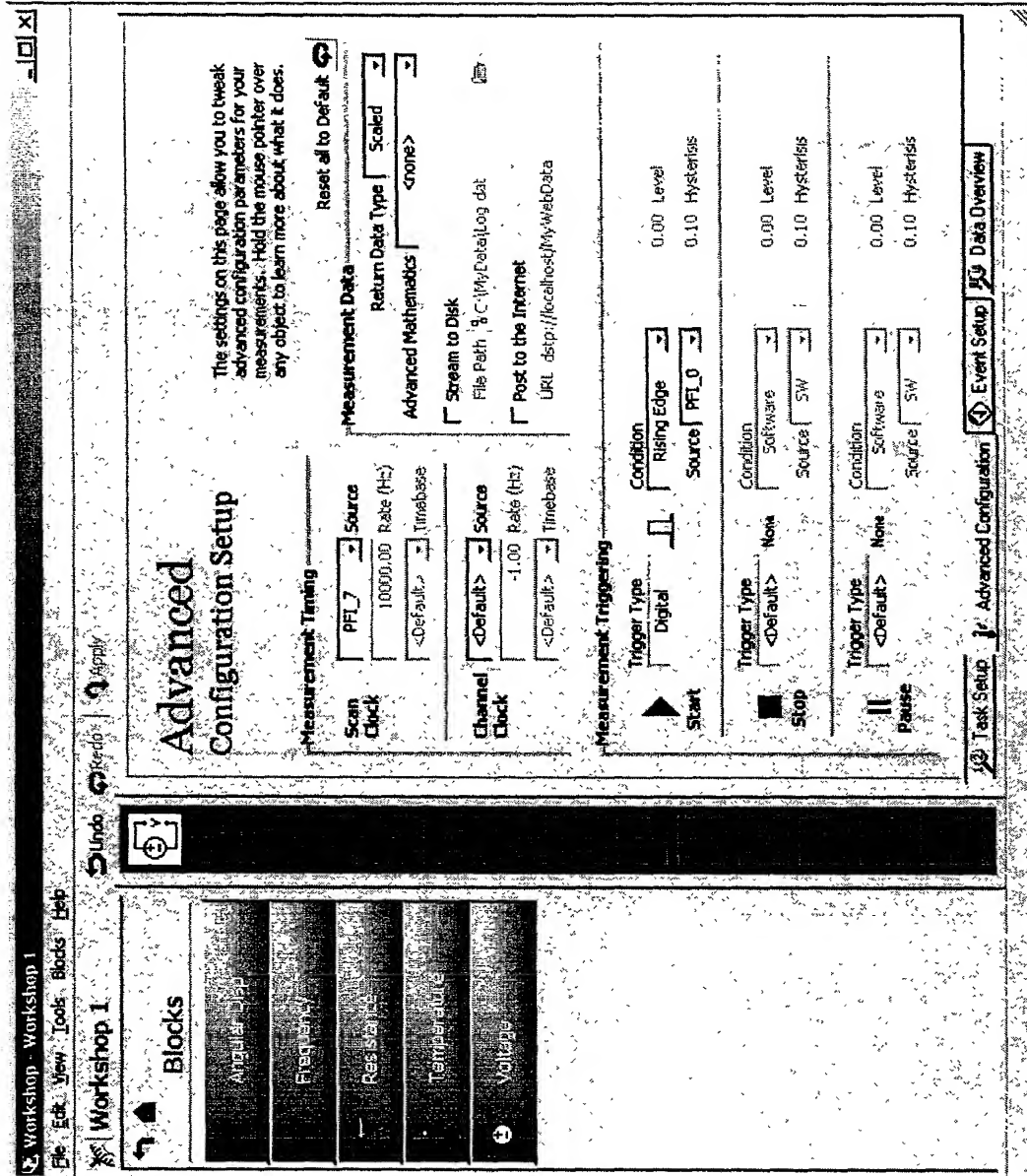
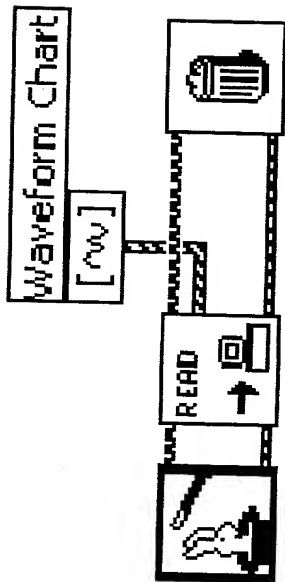
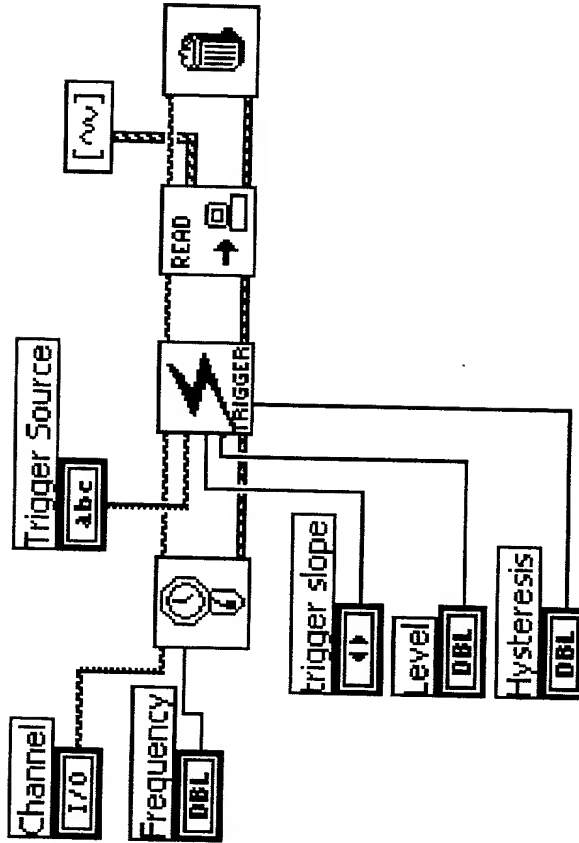


FIG. 43C



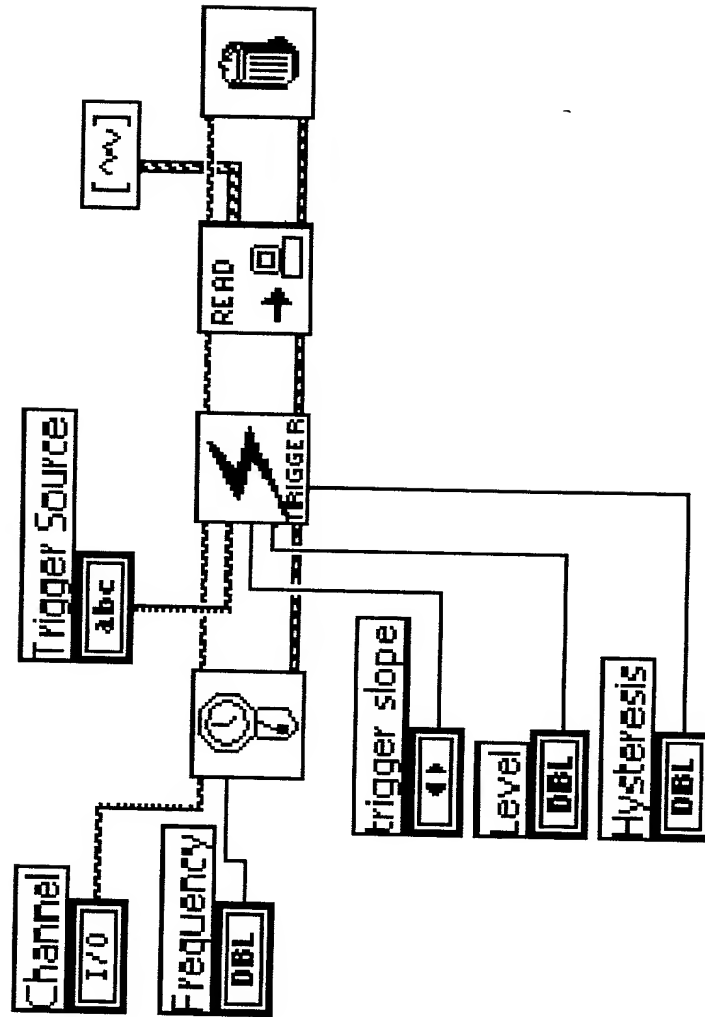
Acquire N Scans External Scan Clock Digital Trigger

FIG. 43D



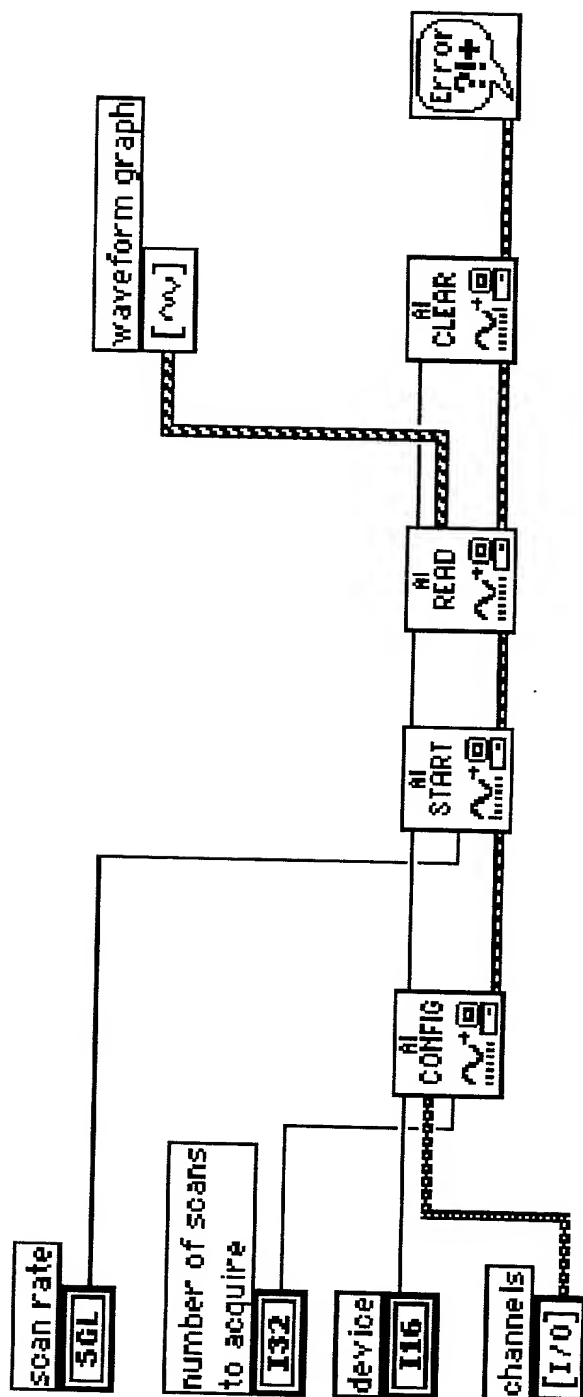
Triggered Acquisition With E-Series Device

FIG. 44A



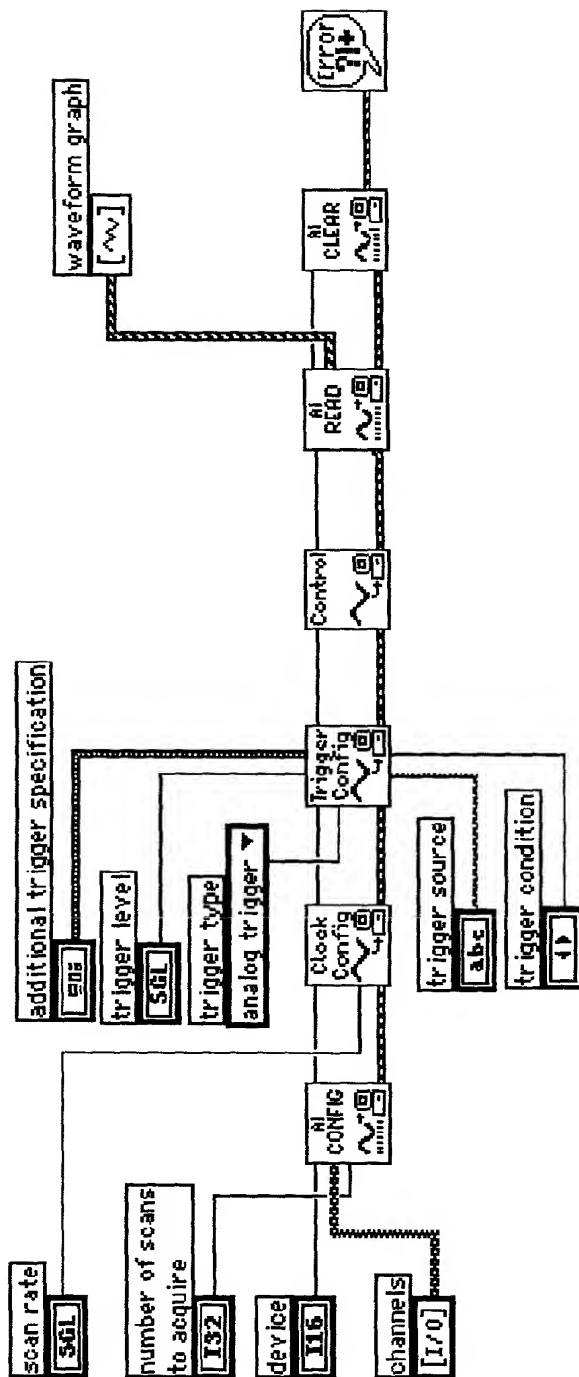
Triggered Acquisition With High Speed Digitizer

FIG. 44B



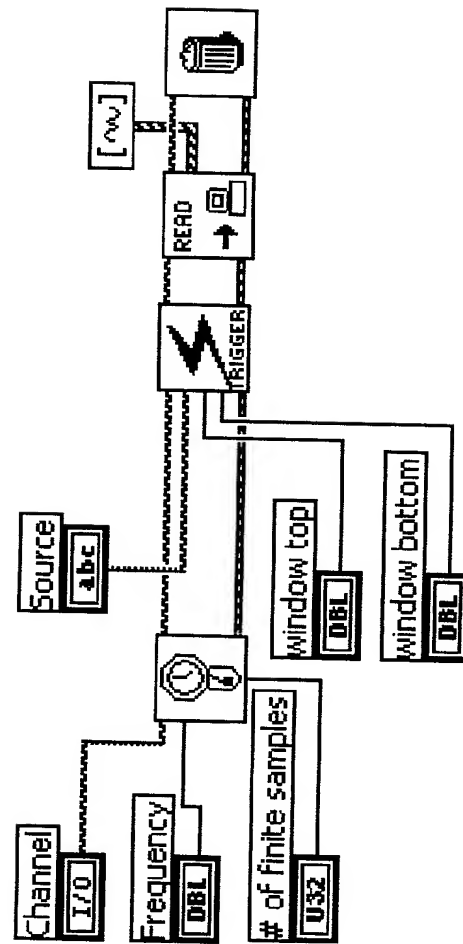
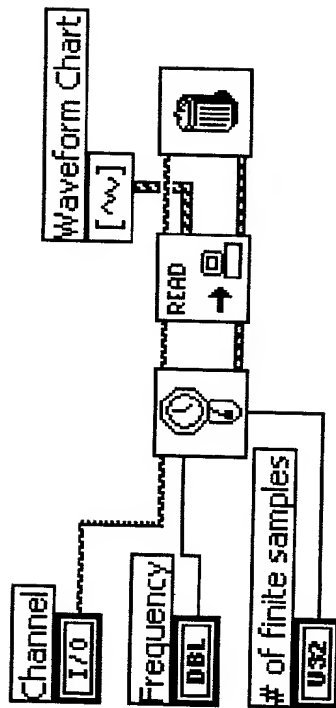
Intermediate Layer (Prior Art)

FIG. 45A



Changes For Analog Window Triggering (Prior Art)

FIG. 45B



Analog Window Triggering

FIG. 45C